TESTING FOR THE VERIFICATION OF COMPLIANCE OF PV INVERTER WITH :

ENGINEERING RECOMMENDATION G59 ISSUE 3 AMENDMENT 2 SEPTEMBER 2015,

RECOMMENDATIONS FOR THE CONNECTION OF GENERATING PLANT TO THE DISTRIBUTION SYSTEM OF LICENSED DISTRIBUTION NETWORK OPERATORS

Procedure: PE.T-LE-62

Test Report Number ..... :	**2217 / 1094 – 9**
Type ..... :	
Tested Model ..... :	**SOFAR 6KTLM-G2**
Variant Models ..... :	**SOFAR 5KTLM-G2, SOFAR 4.6KTLM-G2, SOFAR 4KTLM-G2, SOFAR 3.6KTLM-G2, SOFAR 3KTLM-G2**

APPLICANT

Name ..... :	SGS Tecnos S.A. (Certification Body)
Address ..... :	C/ Trespaderne, 29 - Edificio Barajas 1 28042 MADRID (Spain)
Hired by ..... :	Shenzhen SOFARSOLAR Co., Ltd.
Address ..... :	5/F,Building 4, Antongda Industrial Park, No. 1 Liuxian Avenue, Xin'an Street, Bao'an District, Shenzhen City, Guangdong Province, P.R. China

TESTING LABORATORY

Name ..... :	SGS Tecnos, S.A. (Electrical Testing Laboratory)
Address ..... :	C/ Trespaderne, 29 - Edificio Barajas 1 28042 MADRID (Spain)
Conducted (tested) by ..... :	Roger Hu (Project Engineer)
Approved by ..... :	Omar Kalim (Technical Reviewer)
	Fernando Montes (Laboratory Technical Manager)
Date of issue ..... :	01/03/2018
Number of pages ..... :	101

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Test Report Historical Revision:

Test Report Version	Date	Resume
2217 / 1094 – 9	01 / 03 / 2018	First issuance

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1 SCOPE

SGS Tecnos, S.A. (Electrical Testing Laboratory) has been contract by SGS Tecnos, S.A. (Certification Body), in order to perform the testing according the “Engineering Recommendation G59 Issue 3 Amendment 2 September 2015, Recommendations for the connection of generating plant to the distribution system of licensed distribution network operator”.

2 GENERAL INFORMATION

2.1 TESTING PERIOD AND CLIMATIC CONDITIONS

The necessary testing has been performed along 12 working days between the 30th of November and the 17th of December of 2017.

All the tests and checks have been performed at 25 ± 5ºC, 96 kPa ± 10 kPa and 40% RH ± 10% RH).

SITE TEST

Name.....: Shenzhen SOFARSOLAR Co., Ltd.

Address .....: 5/F,Building 4, Antongda Industrial Park, No. 1 Liuxian Avenue, Xin'an Street, Bao'an District, Shenzhen City, Guangdong Province, P.R. China

2.2 EQUIPMENT UNDER TESTING

Apparatus type ..... : Solar Grid-tied Inverter

Installation ..... : Fixed (permanent connection)

Manufacturer ..... : Shenzhen SOFARSOLAR Co., Ltd.

Trade mark..... : SOFAR SOLAR

Model / Type reference ..... : SOFAR 6KTLM-G2

Serial Number ..... : ZG1ES060H61001

Software Version..... : V0.22

Rated Characteristics..... : DC input: 90-580V, 11/11A
AC output: 230V, 50Hz, 27.3A, 6000VA

Date of manufacturing: 2017

Test item particulars

Input ..... : 90-580V, 11/11A

Output..... 230V, 50Hz, 27.3A, 6000VA

Class of protection against electric shock... : Class I

Degree of protection against moisture ..... : IP 65

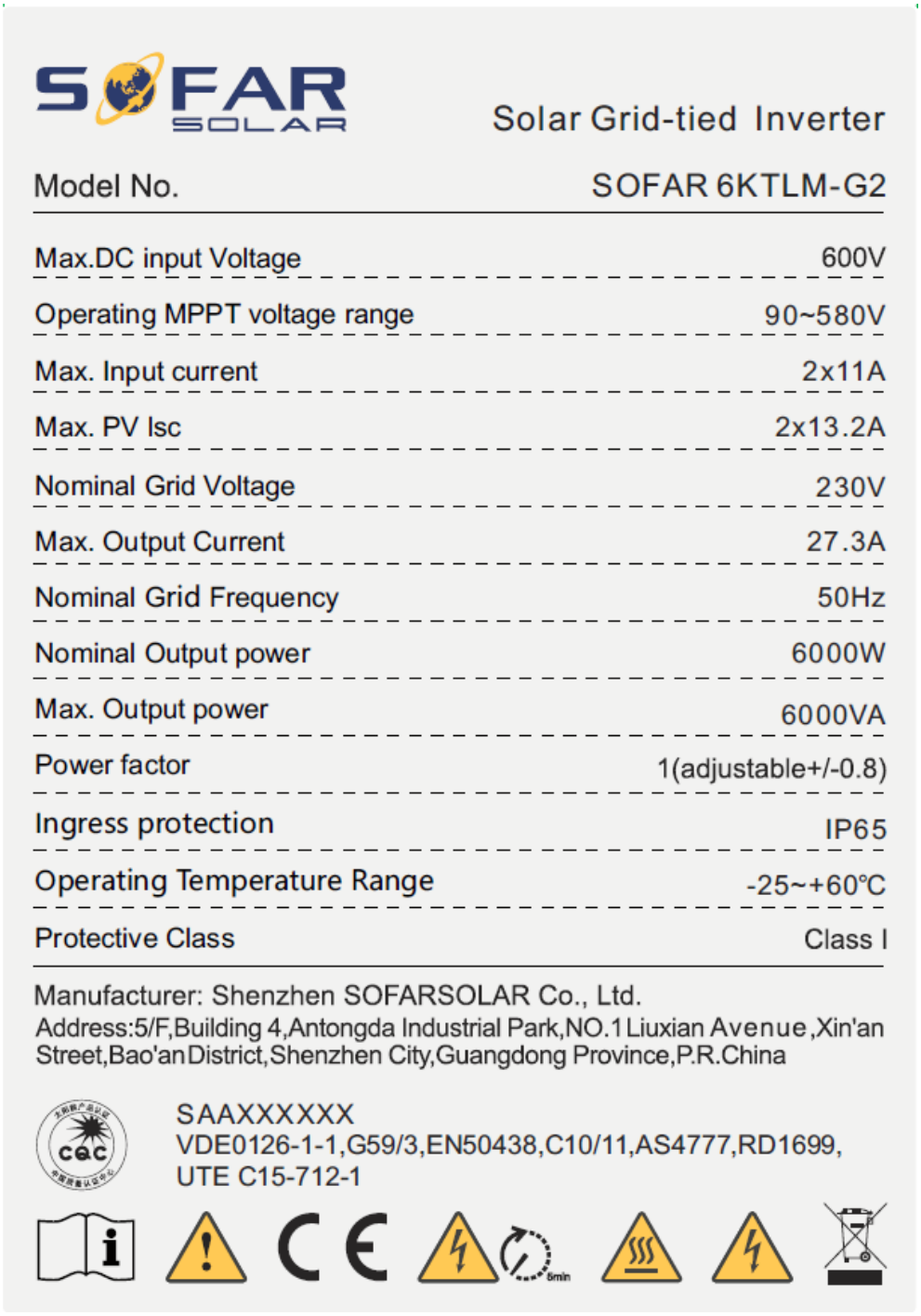
Type of connection to the main supply ..... : TN

Cooling group..... : Heat sink

Modular ..... : No

Internal Transformer..... : No

Copy of marking plate (representative):



Note:

1. The above markings are the minimum requirements required by the safety standard. For the final production samples, the additional markings which do not give rise to misunderstanding may be added.
2. Label is attached on the side surface of enclosure and visible after installation
3. Labels of other models are as the same with SOFAR 6KTLM-G2's except the parameters of rating.

Equipment Under Testing:

- **SOFAR 6KTLM-G2**

The variants models are:

- **SOFAR 5KTLM-G2,**
- **SOFAR 4.6KTLM-G2,**
- **SOFAR 4KTLM-G2,**
- **SOFAR 3.6KTLM-G2,**
- **SOFAR 3KTLM-G2**

The variants models have been included in this test report without tests because the following features don´t change regarding to the tested model:

- Same connection system and hardware topology
- Same control algorithm.
- Output power within 2,5 and 2/3 of the EUT or Modular inverters.
- Same Firmware Version

The results obtained apply only to the particular sample tested that is the subject of the present test report. The most unfavorable result values of the verifications and tests performed are contained herein. Throughout this report a point ~~(comma)~~ is used as the decimal separator.

2.3 TEST EQUIPMENT LIST

No.	Equipment Name	MARK/Model No.	Equipment No.	Equipment calibration due date
1	Digital oscilloscope	Agilent / DSO5014A	MY50070288	2018-02-15
2	Current clamp	FLUKE / i1000s	30413441	2018-02-15
3	Differential probe	Sanhua / SI-9110	111134	2018-02-15
4	Power analyzer	ZLG / PA3000	PA3005-P0005-1246	2018-02-15
5	Temperature & Humidity meter	VICTOR / VC230A	WS01	2018-09-03
6	Power analyzer	YOKOGAWA / WT 3000	EP-011	2018-08-05
7	Digital oscilloscope	YOKOGAWA/DL 850	EP-001	2018-10-22
No.	**Equipment Name**	**MARK/Model No.**	**SGS CODE (DIE)**	**Equipment calibration due date**
8	Multimeter	FLUCKE / 289	DIE.560040	02/11/2018
9	Current Clamp	HIOKI / 3285	DIE.510051	06/02/2018

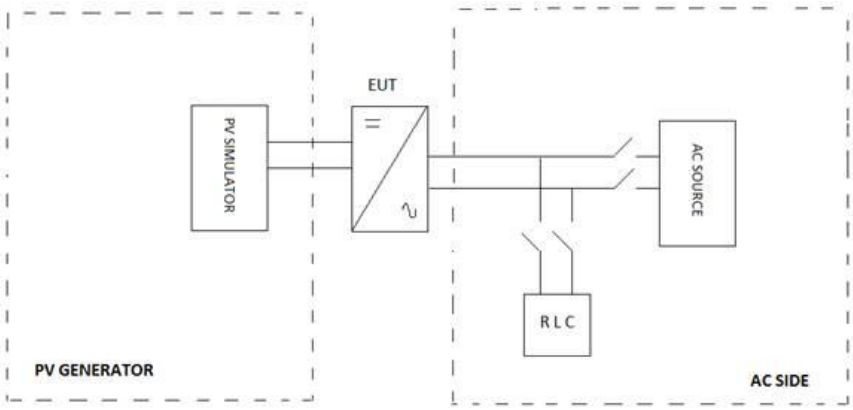
2.4 MEASUREMENT UNCERTAINTY

Associated uncertainties through measurements showed in this this report are the maximum allowable uncertainties.

Magnitude	Uncertainty
Voltage measurement	±1.5 %
Current measurement	±2.0 %
Frequency measurement	±0.2 %
Time measurement	±0.2 %
Power measurement	±2.5 %
Phase Angle	±1º
Temperature	±3º C
Note1: Measurements uncertainties showed in this table are maximum allowable uncertainties. The measurement uncertainties associated with other parameters measured during the tests are in the laboratory at disposal of the solicitant.	

2.5 TEST SET UP OF THE DIFFERENT STANDARD

Below is the simplified construction of the test set up.



Different equipment has been used to take measures as it shows in chapter 2.3. Current and voltage clamps have been connected to the inverter input / output for all the tests.
All the tests described in the following pages have used this specified test setup.

The test bench used includes:

EQUIPMENT	MARK / MODEL	RATED CHARACTERISTICS	OWNER / ID.CODE
AC source	Chroma / 61860	100KVA 10-300Vrms 45-65Hz	--
DC source	Chroma / 62150H-1000S	0 – 1000Vdc (0.01V step) 0 – 40A (0.01A step)	--

2.6 Definitions

EUT	Equipment Under Testing	Hz	Hertz
A	Ampere	V	Volt
VAr	Volt-Ampere reactive	W	Watt
EMC	Electromagnetic Compatibility	p.u	Per unit
Un	Nominal Voltage	Pn	Nominal Active Power
In	Nominal Current	Qn	Nominal Reactive Power
Ia	Active Current	Sn	Nominal Apparent Power
Ir	Reactive Current	THD	Total Harmonic Distortion
I_h	Harmonic Current	TDD	Total Demand Distortion
PST	Severity of Flicker Short-Term	PLT	Severity of Flicker Long-Term
dc	Maximum Variation of Voltage	d(t)	Variation of Voltage
d max	Maximum Absolute Value of Voltage Variation	MPS	Medium Power Station

3 RESUME OF TEST RESULTS

INTERPRETATION KEYS

Test object does meet the requirement ..... **P** Pass
Test object does not meet the requirement ..... **F** Fails
Test case does not apply to the test object ..... **N/A** Not applicable
To make a reference to a table or an annex. ..... See additional sheet
To indicate that the test has not been realized ..... **N/R** Not realized

STANDAARD CLAUSE	STANDARD REQUIREMENTS G59 Issue 3 Amendment 2: 2015 TEST	REMARKS	RESULT
13.8.3	**Functional Testing**		**P**
13.8.3.1	Disconnection Times		P
13.8.3.2	Over/Under Voltage		P
13.8.3.3	Over/Under Frequency		P
13.8.3.4	Loss of Mains		P
13.8.3.5	Reconnection		P
13.8.3.6	Frequency drift and step change stability		P
13.8.4	**Power Quality**		**P**
13.8.4.1	Harmonics		P
13.8.4.2	Power Factor		P
13.8.4.3	Voltage Flicker		P
13.8.4.4	DC Injection		P
13.8.4.6	Short circuit current contribution		P
13.8.4.7	Self-Monitoring solid state	No solid state switching devices	N/A
13.8.4.8	Electromagnetic Compatibility		P

Note: The declaration of conformity has been evaluated taking into account the IEC Guide 115.

4 TEST RESULTS

4.1 FUNCTIONAL TESTING

4.1.1 Disconnection Times

This test has been done according to the point 13.8.3.1 of the standard.

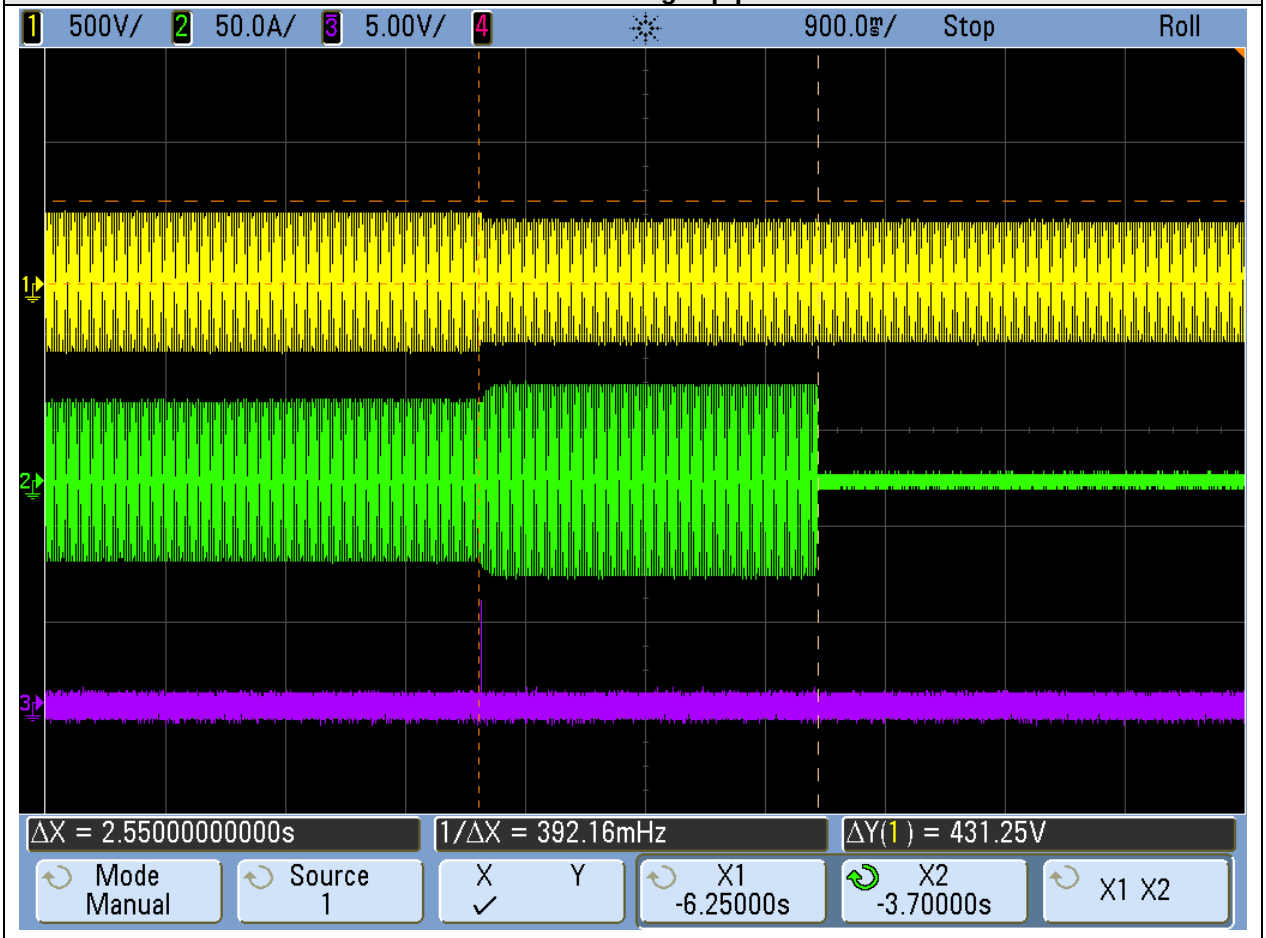
The results are shown on points 4.1.2.2 and 4.1.3.2 where times represented include delay time plus trip time. No trip time shall exceed the maximum trip time which is delay time plus 0.5s.

This test has been done performing two different tests:

- Trip voltage or frequency test, to asses that the protection function of the inverter works as the voltage and frequency levels stated by the standard.
- Trip time test, to asses that the disconnection of the inverter takes place into the time limits established by the standard.

Following indications shall be taken into account to for test results offered.

Information relating trip pictures



Ch1: AC Output voltage
Ch2: AC Output current
Ch3: Trip signal

4.1.2 Over/ Under Voltage

4.1.2.1 Trip value test.

Tests have been done according to the point 13.8.3.2 of the standard, as the following procedure:

- For undervoltage protection: Starting from a voltage level 2%Un above the trip value of the protection function to be tested, the voltage is decreased 0,5%Un in steps of at least 150% of the trip time delay stated in the protection function to be tested.

- For overvoltage protection: Starting from a voltage level 2%Un below the trip value of the protection function to be tested, the voltage is increased 0,5%Un in steps of at least 150% of the trip time delay stated in the protection function to be tested.

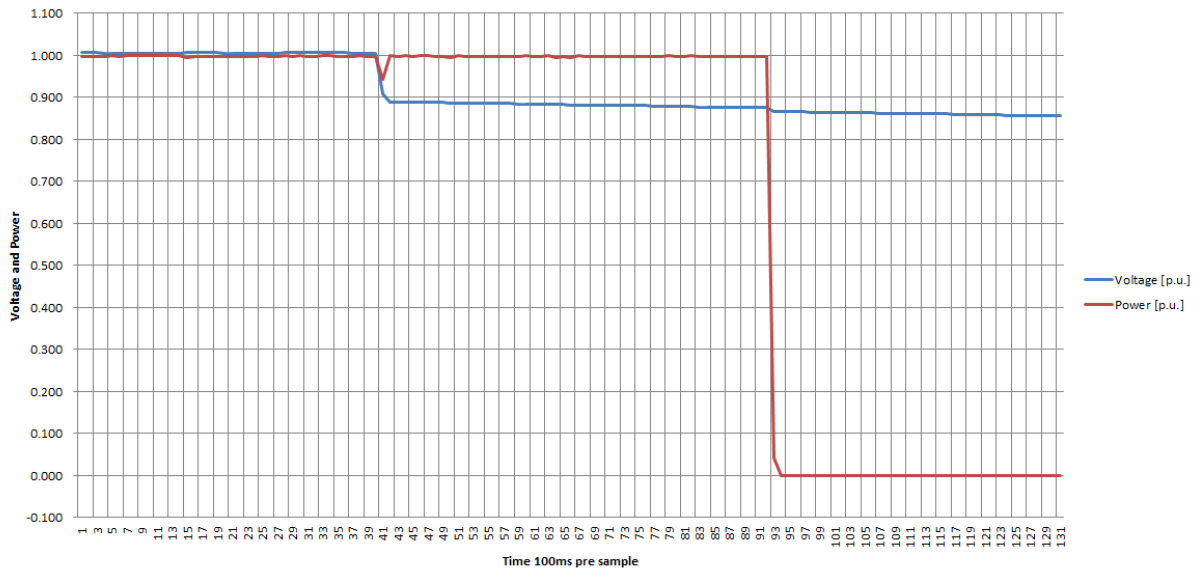
Maximum deviation allowed in voltage trip value is ±1,5% Un. Trips have been repeated 5 times at each voltage level.

Following tables show the test results:

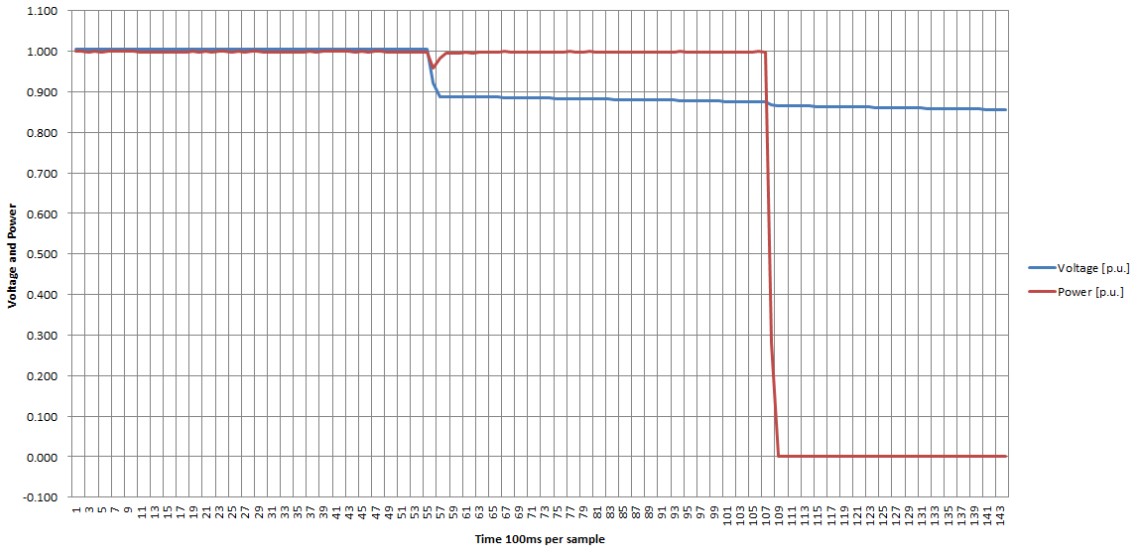
Stage/Prot Function	Test	Voltage at the start (V)	Trip Voltage Desired (V)	Trip voltage measured (V)	Disconnection	Deviation measured (%Un)
U/V st1 87% Un	1	230	200.10	199.22	☐ NO ☒ YES	-0.383
	2	230	200.10	199.26	☐ NO ☒ YES	-0.365
	3	230	200.10	199.42	☐ NO ☒ YES	-0.296
	4	230	200.10	199.36	☐ NO ☒ YES	-0.322
	5	230	200.10	199.13	☐ NO ☒ YES	-0.422
U/V st2 80% Un	1	230	184.00	183.92	☐ NO ☒ YES	-0.035
	2	230	184.00	183.97	☐ NO ☒ YES	-0.013
	3	230	184.00	184.01	☐ NO ☒ YES	0.004
	4	230	184.00	183.98	☐ NO ☒ YES	-0.009
	5	230	184.00	184.08	☐ NO ☒ YES	0.035
O/V st1 114% Un	1	230	262.20	262.84	☐ NO ☒ YES	0.278
	2	230	262.20	262.59	☐ NO ☒ YES	0.170
	3	230	262.20	262.93	☐ NO ☒ YES	0.317
	4	230	262.20	262.64	☐ NO ☒ YES	0.191
	5	230	262.20	262.58	☐ NO ☒ YES	0.165
O/V st2 119% Un	1	230	273.70	273.90	☐ NO ☒ YES	0.087
	2	230	273.70	273.93	☐ NO ☒ YES	0.100
	3	230	273.70	273.98	☐ NO ☒ YES	0.122
	4	230	273.70	273.95	☐ NO ☒ YES	0.109
	5	230	273.70	274.01	☐ NO ☒ YES	0.135

Test results are graphically shown in following pages.

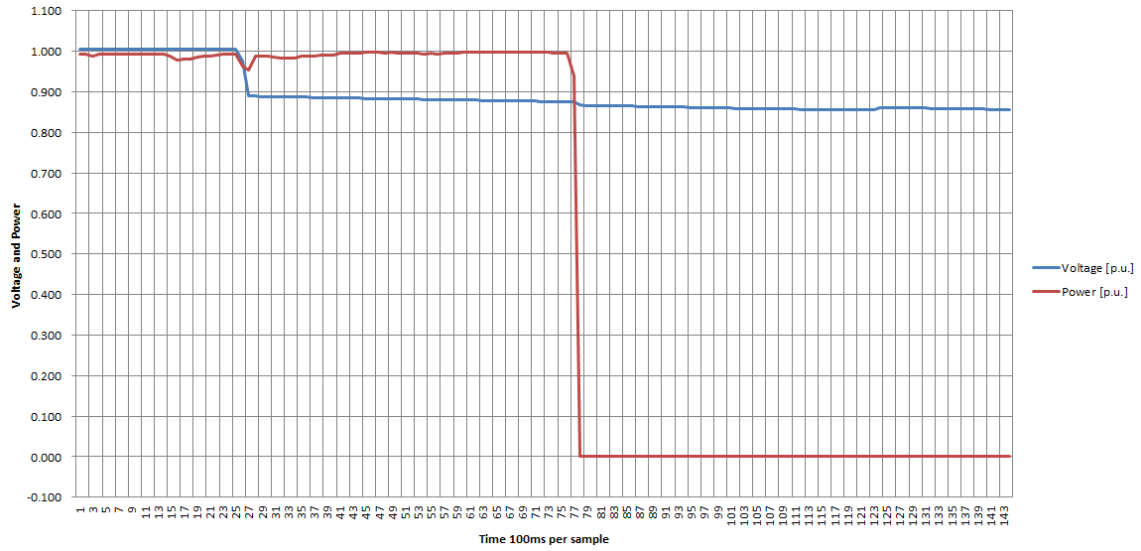
Under voltage, Stage 1 - Test 1



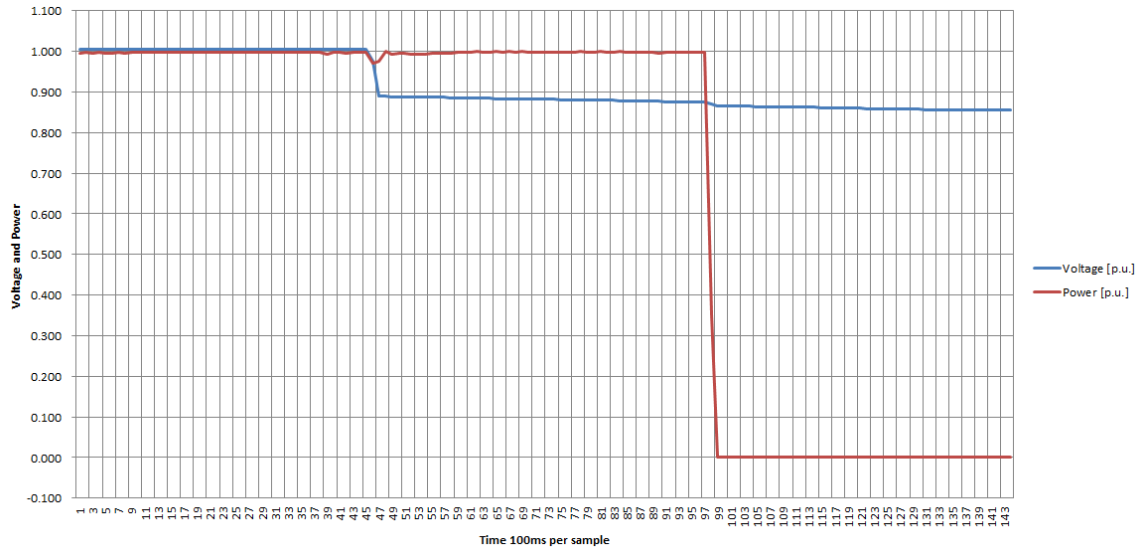
Under voltage, Stage 1 - Test 2



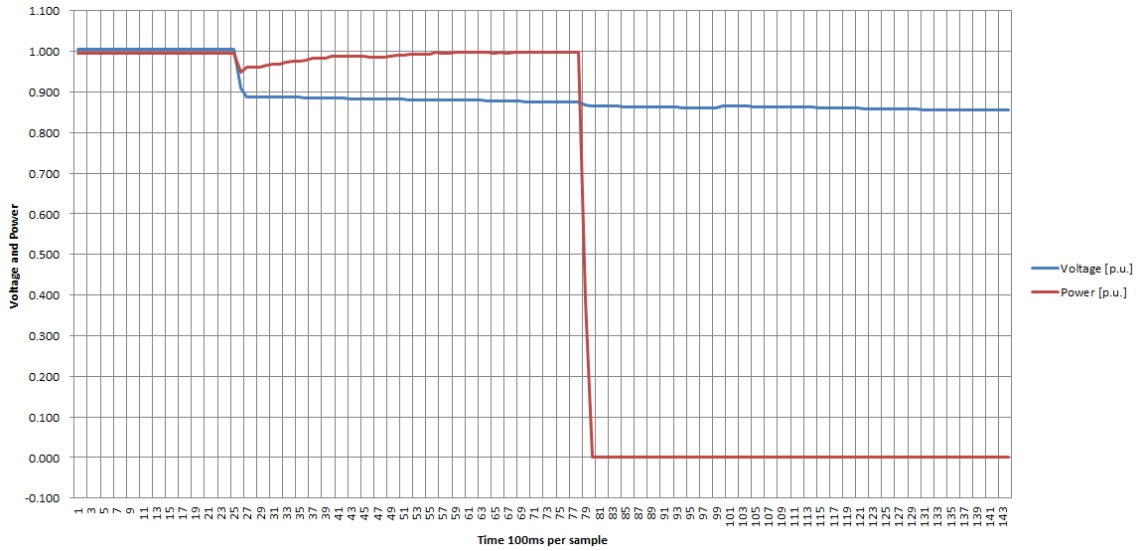
Under voltage, Stage 1 - Test 3



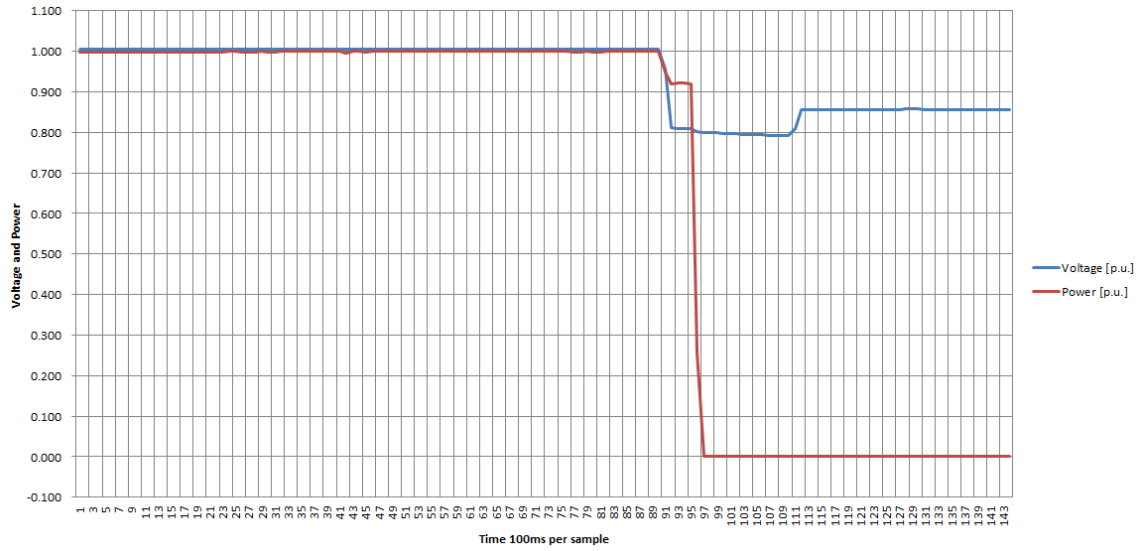
Under voltage, Stage 1 - Test 4



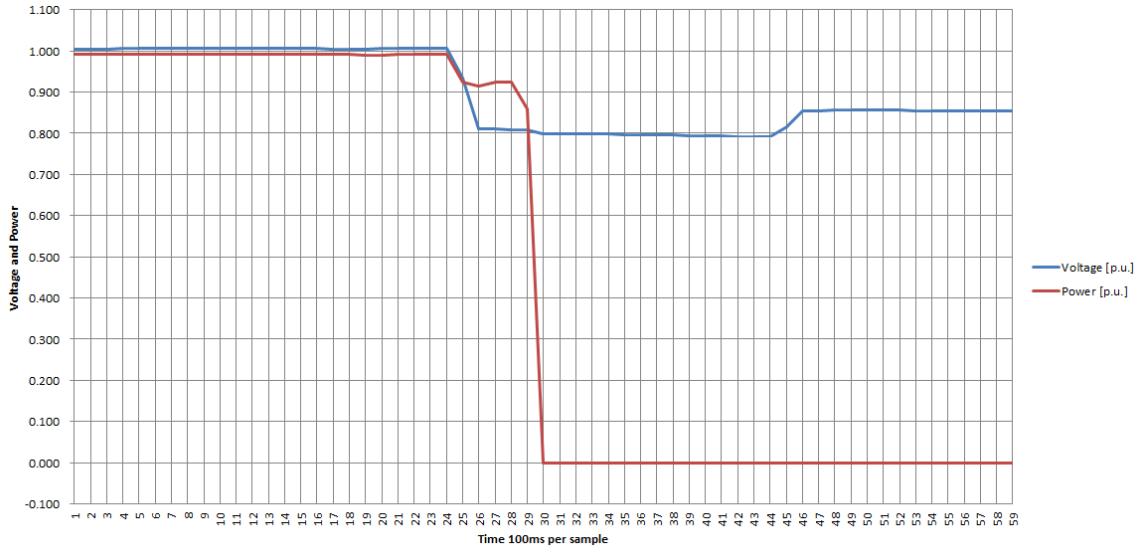
Under voltage, Stage 1 - Test 5



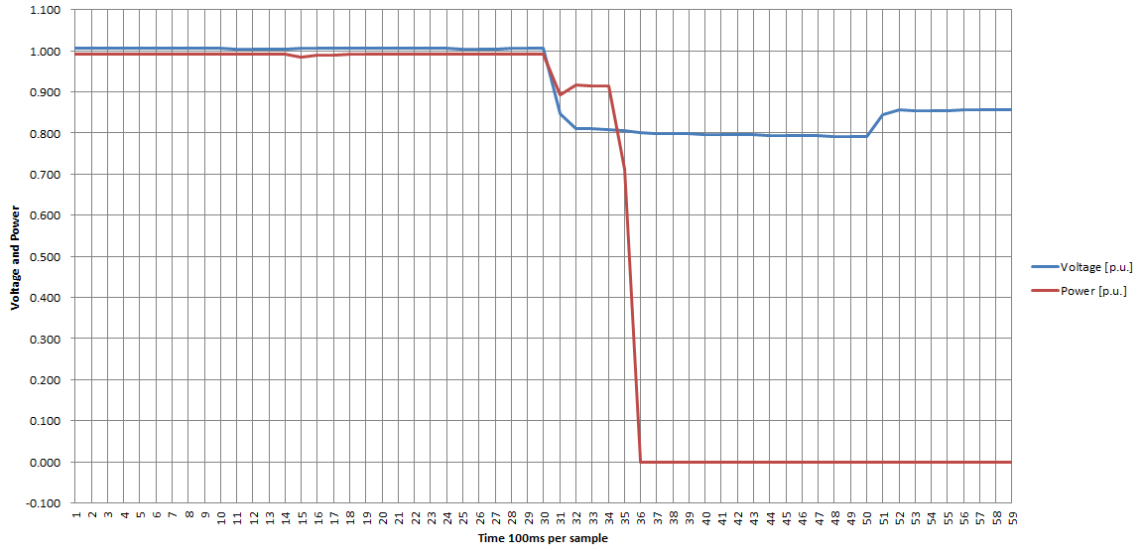
Under voltage, Stage 2 - Test 1



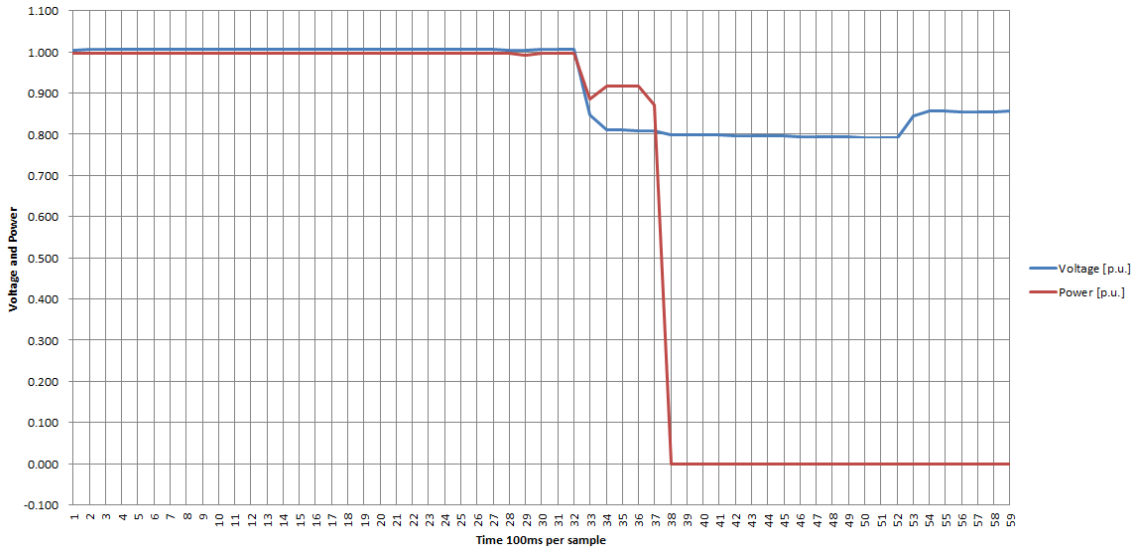
Under voltage, Stage 2 - Test 2



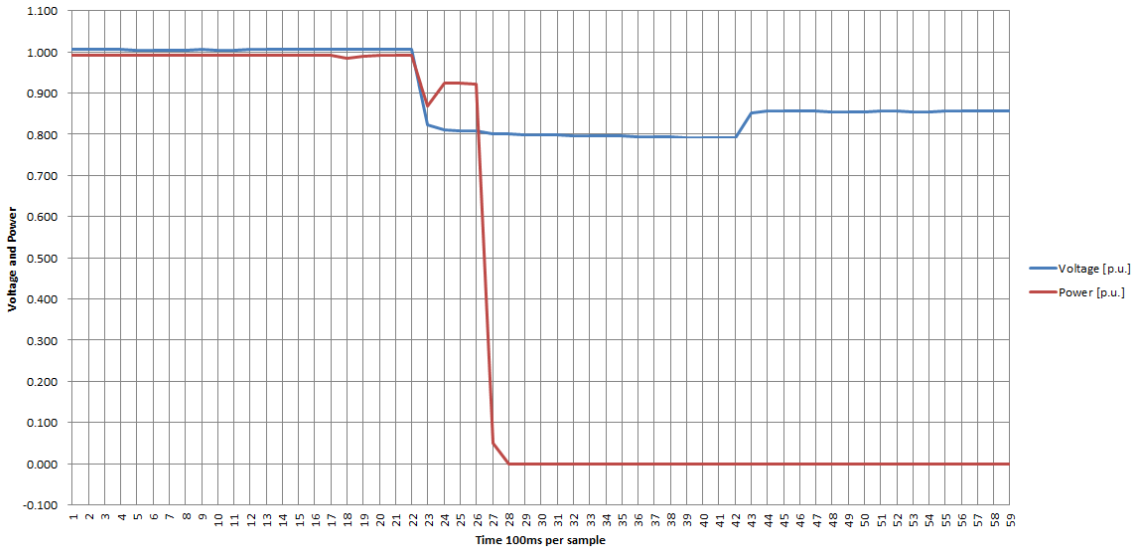
Under voltage, Stage 2 - Test 3



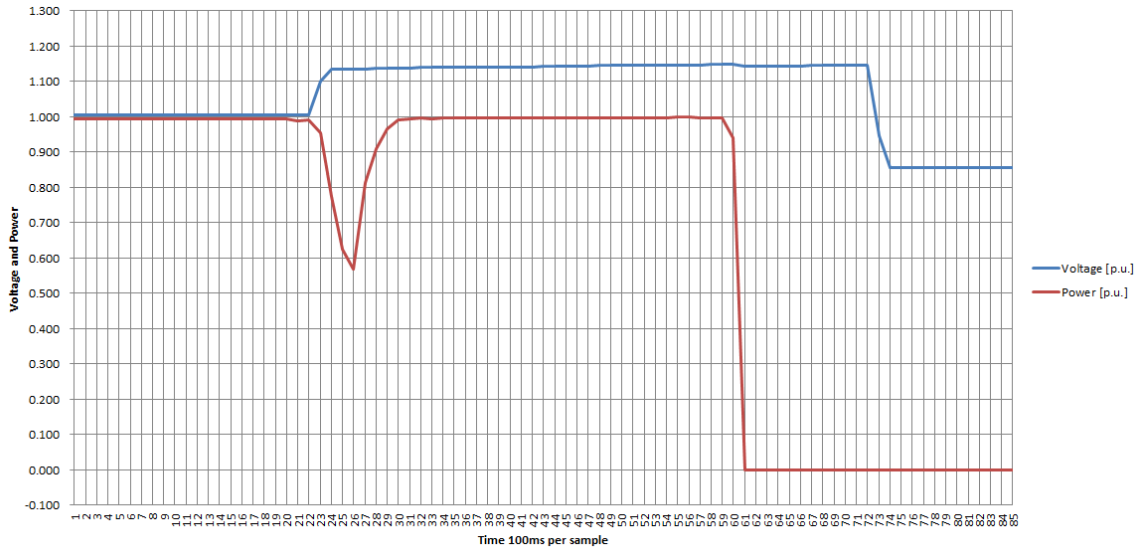
Under voltage, Stage 2 - Test 4



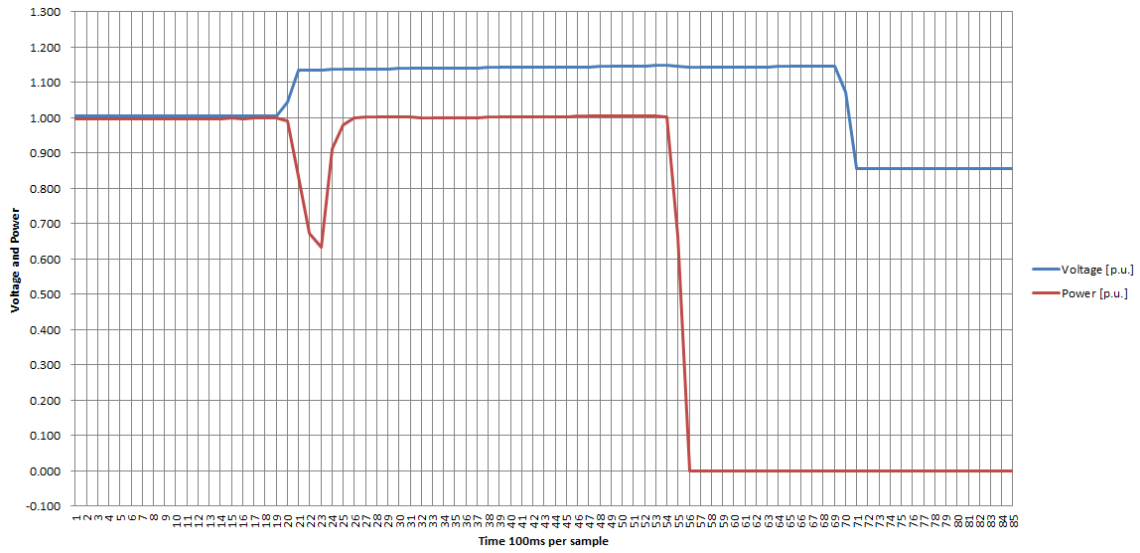
Under voltage, Stage 2 - Test 5



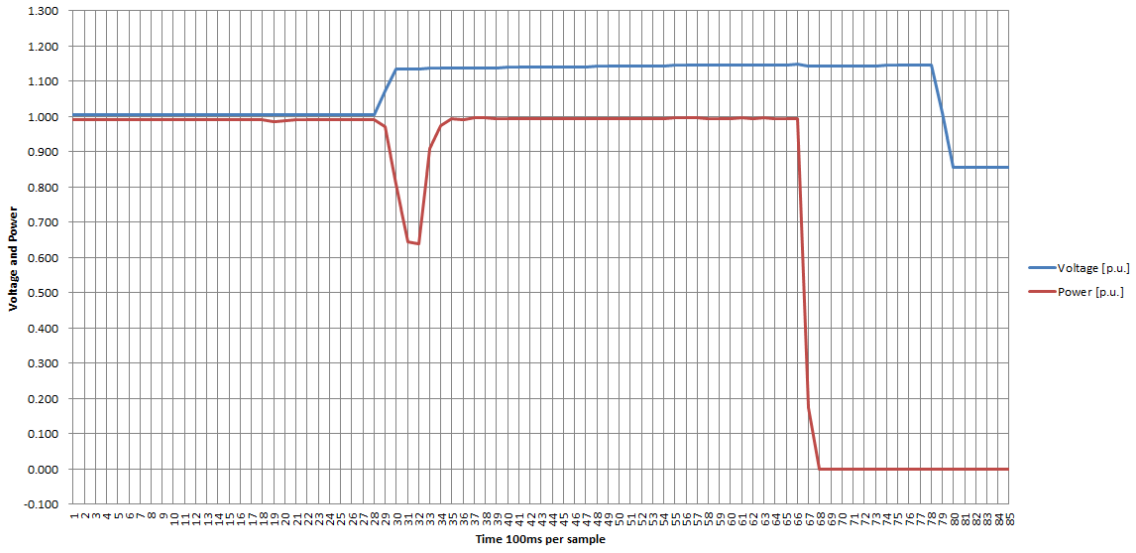
Over voltage, Stage 1 - Test 1



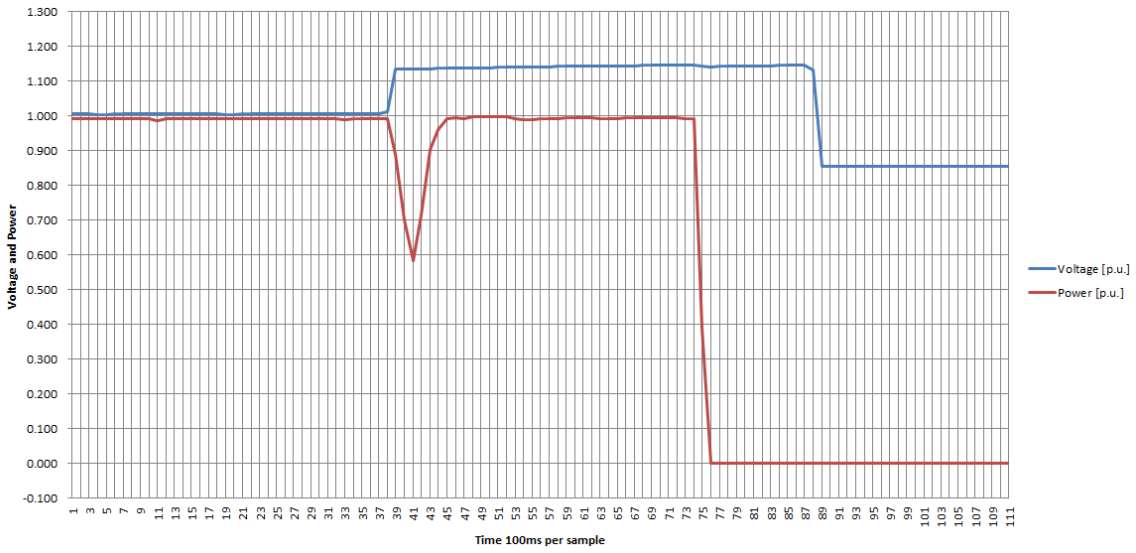
Over voltage, Stage 1 - Test 2



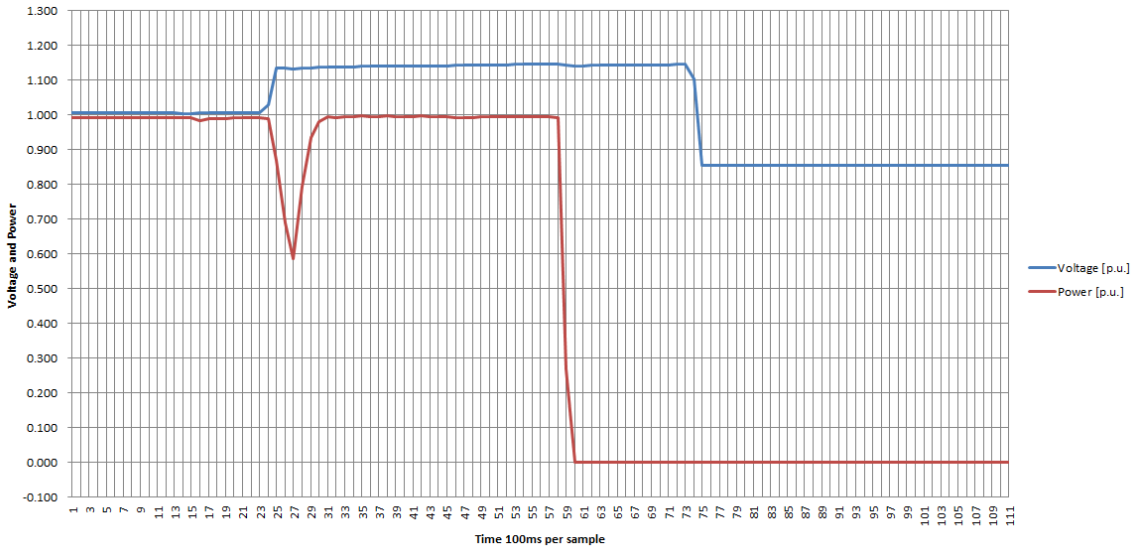
Over voltage, Stage 1 - Test 3



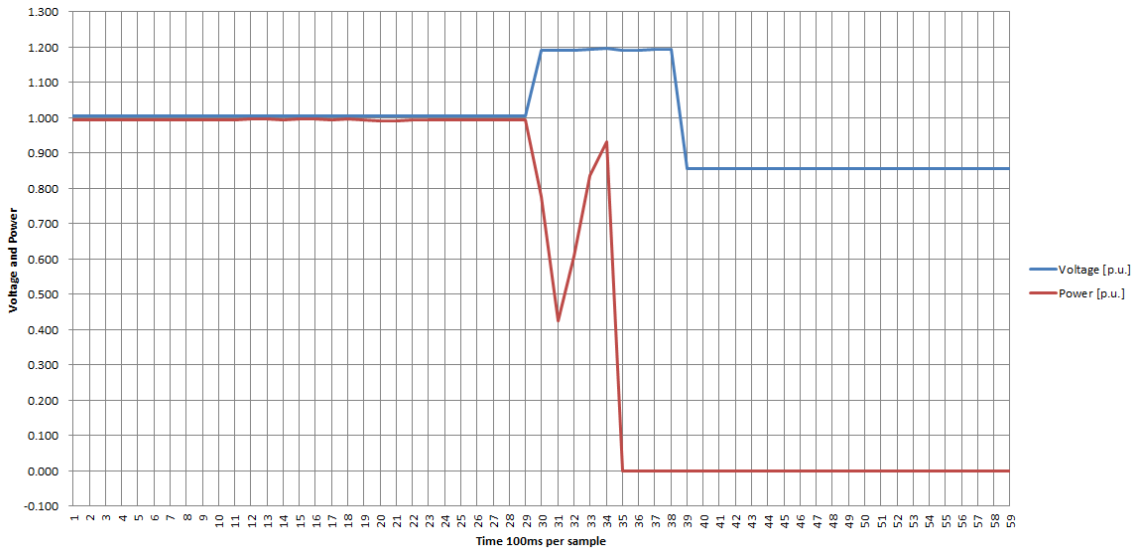
Over voltage, Stage 1 - Test 4



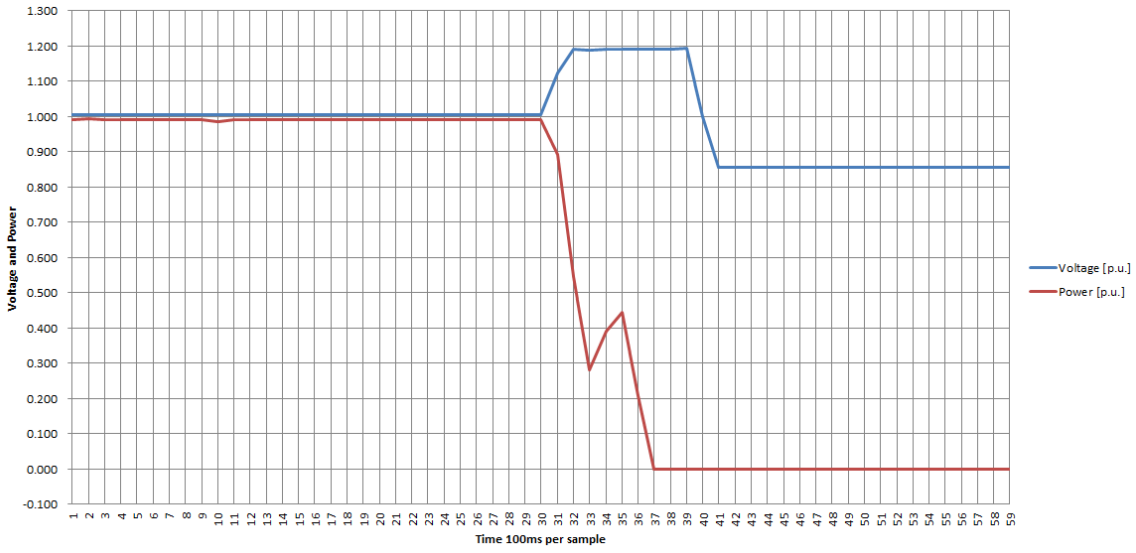
Over voltage, Stage 1 - Test 5



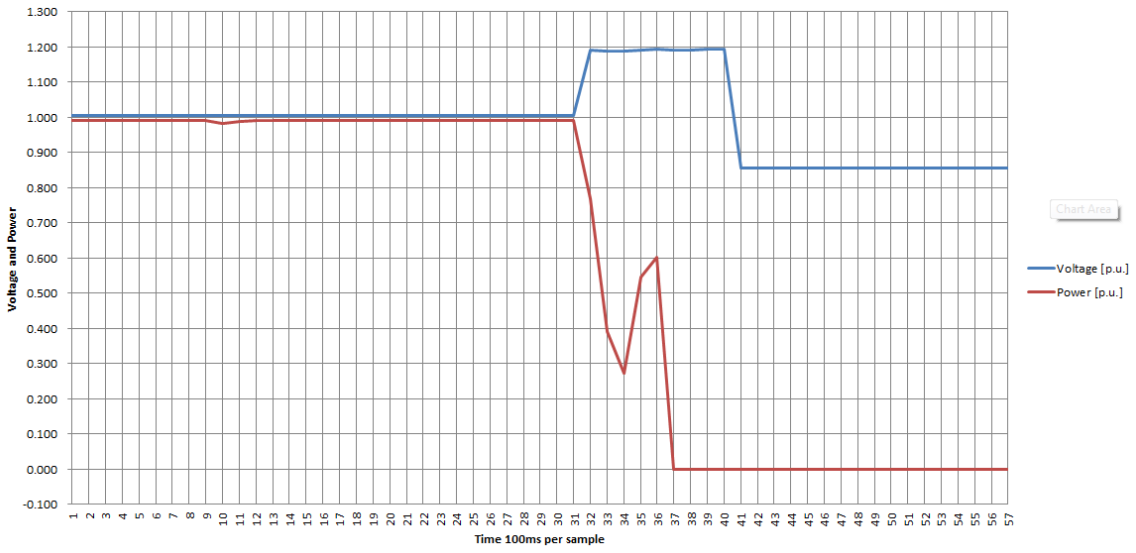
Over voltage, Stage 2 - Test 1



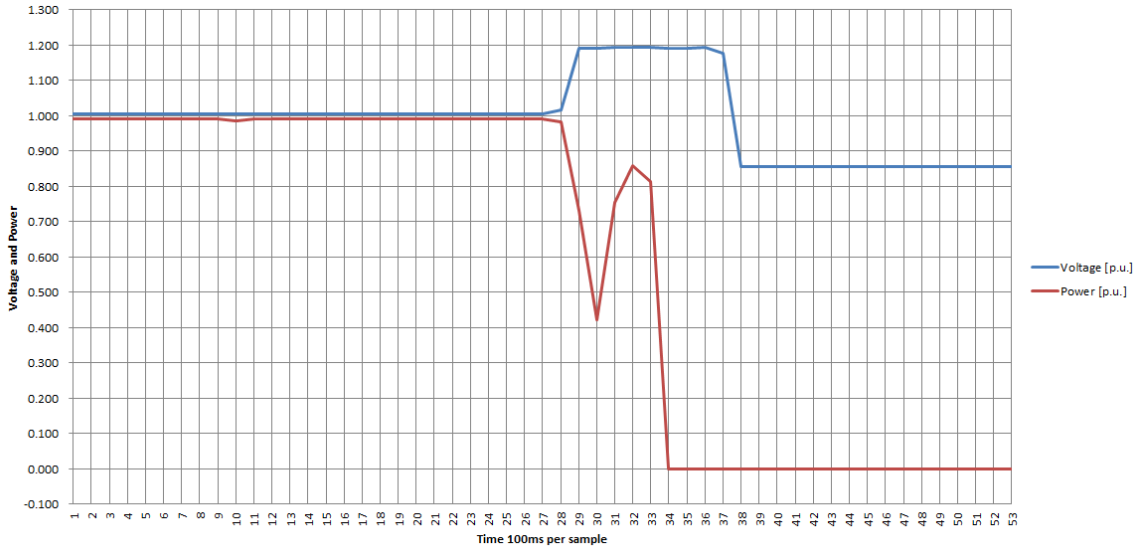
Over voltage, Stage 2 - Test 2



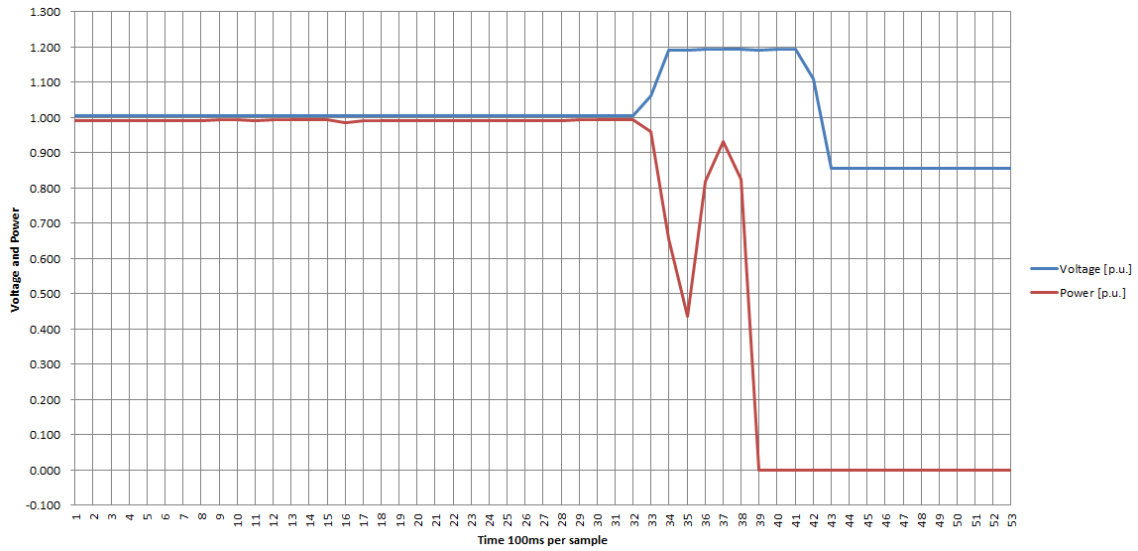
Over voltage, Stage 2 - Test 3



Over voltage, Stage 2 - Test 4



Over voltage, Stage 2 - Test 5



4.1.2.2 Trip time test.

The tests have been made as the following procedure:

- For undervoltage protection: Starting from a voltage level 2%Un above the trip value of the protection function to be tested, the voltage is decreased in a step of 4%Un and it is measured from that instant the time it takes to disconnect.
- For overvoltage protection: Starting from a voltage level 2%Un below the trip value of the protection function to be tested, the voltage is increased in a step of 4%Un and it is measured from that instant the time it takes to disconnect.

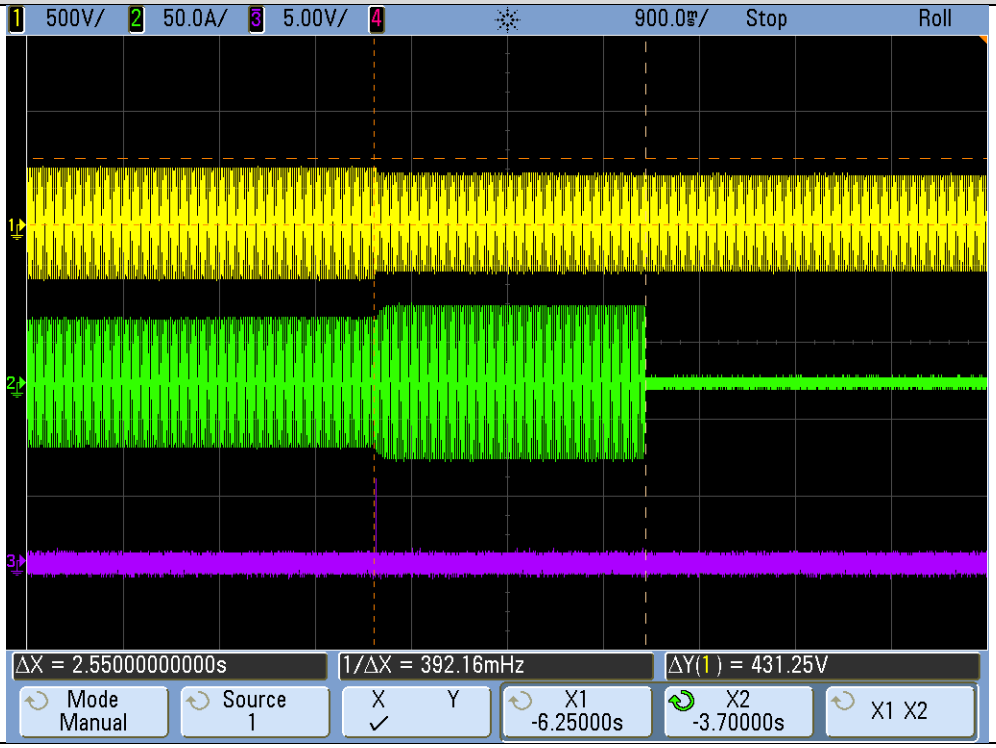
Trips have been repeated 5 times at each voltage level.

Following tables show the test results:

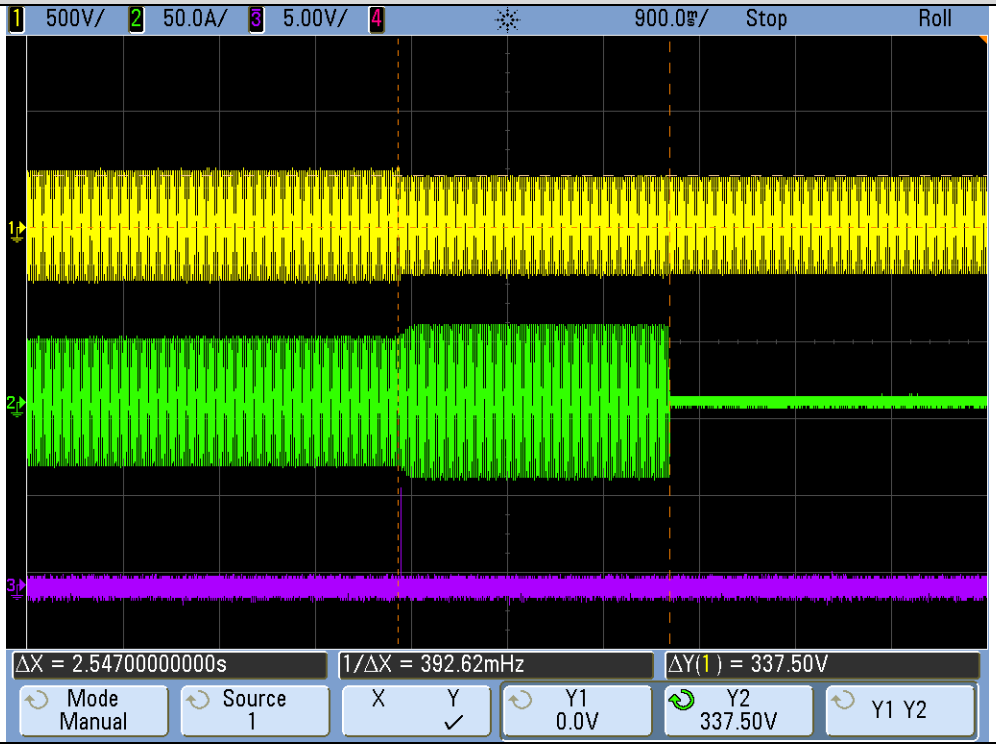
Stage/Prot Function	Test	Delay Time limit (s)	Maximum trip time (s)	Trip time measured (s)	Disconnection
U/V st1 87% Un	1	2.5	3.000	2.550	☐ NO ☒ YES
	2	2.5	3.000	2.547	☐ NO ☒ YES
	3	2.5	3.000	2.556	☐ NO ☒ YES
	4	2.5	3.000	2.547	☐ NO ☒ YES
	5	2.5	3.000	2.556	☐ NO ☒ YES
U/V st2 80% Un	1	0.5	1.000	0.528	☐ NO ☒ YES
	2	0.5	1.000	0.520	☐ NO ☒ YES
	3	0.5	1.000	0.518	☐ NO ☒ YES
	4	0.5	1.000	0.528	☐ NO ☒ YES
	5	0.5	1.000	0.520	☐ NO ☒ YES
O/V st1 114% Un	1	1.0	1.500	1.030	☐ NO ☒ YES
	2	1.0	1.500	1.035	☐ NO ☒ YES
	3	1.0	1.500	1.050	☐ NO ☒ YES
	4	1.0	1.500	1.040	☐ NO ☒ YES
	5	1.0	1.500	1.050	☐ NO ☒ YES
O/V st2 119% Un	1	0.5	1.000	0.520	☐ NO ☒ YES
	2	0.5	1.000	0.530	☐ NO ☒ YES
	3	0.5	1.000	0.532	☐ NO ☒ YES
	4	0.5	1.000	0.528	☐ NO ☒ YES
	5	0.5	1.000	0.520	☐ NO ☒ YES

Test results are graphically shown in following pages.

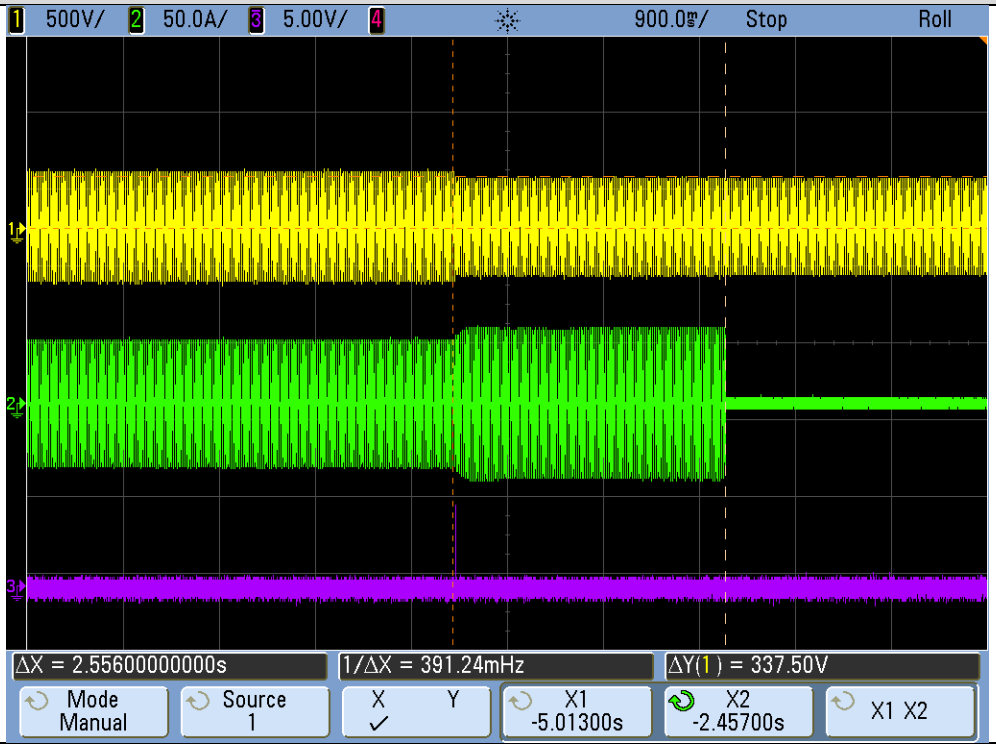
Under voltage, Stage 1 - Test 1



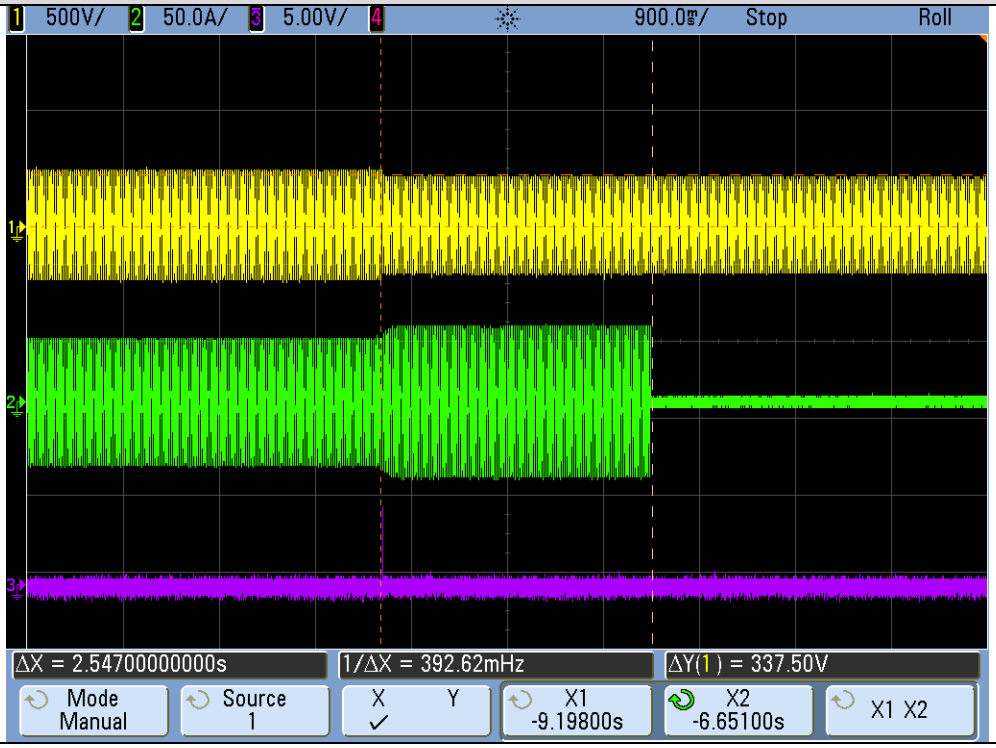
Under voltage, Stage 1 - Test 2



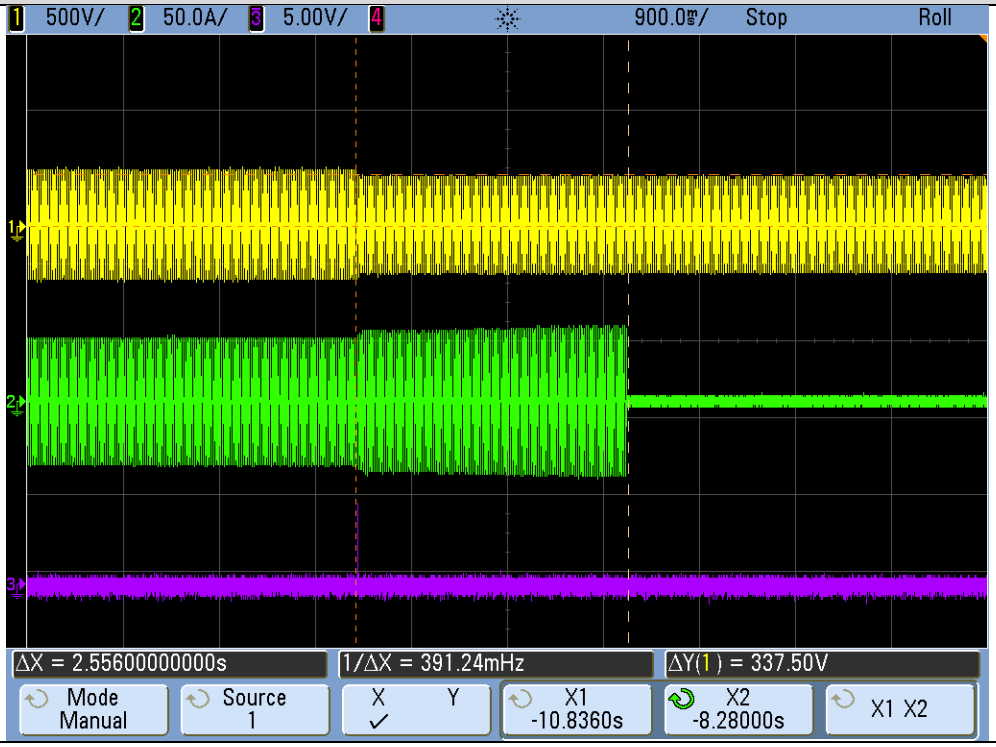
Under voltage, Stage 1 - Test 3



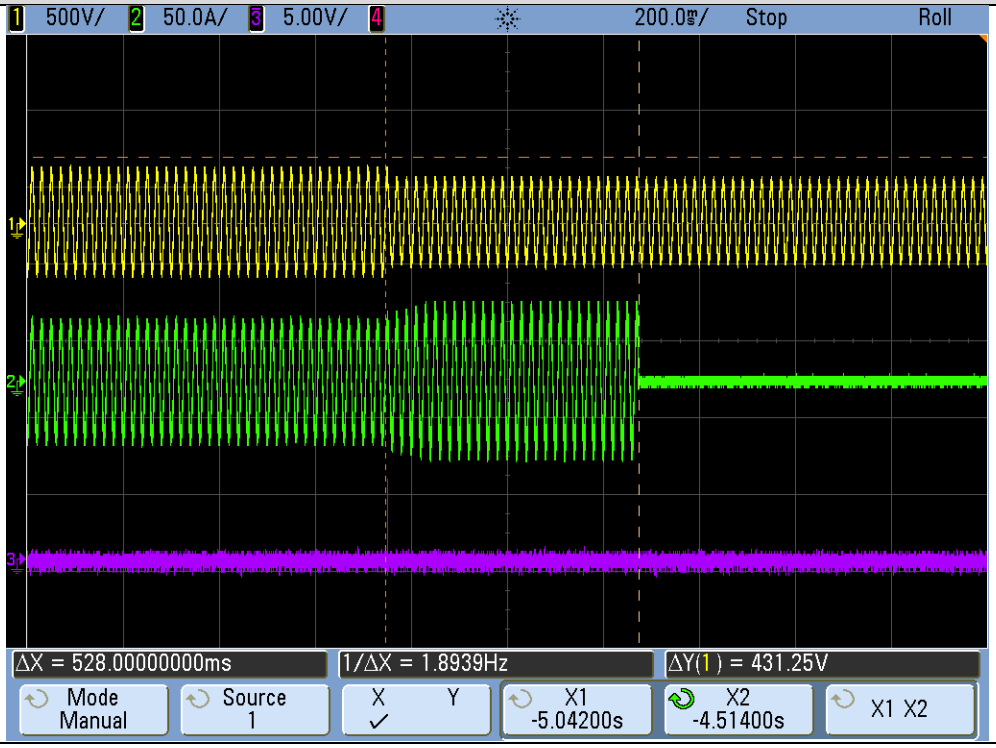
Under voltage, Stage 1 - Test 4



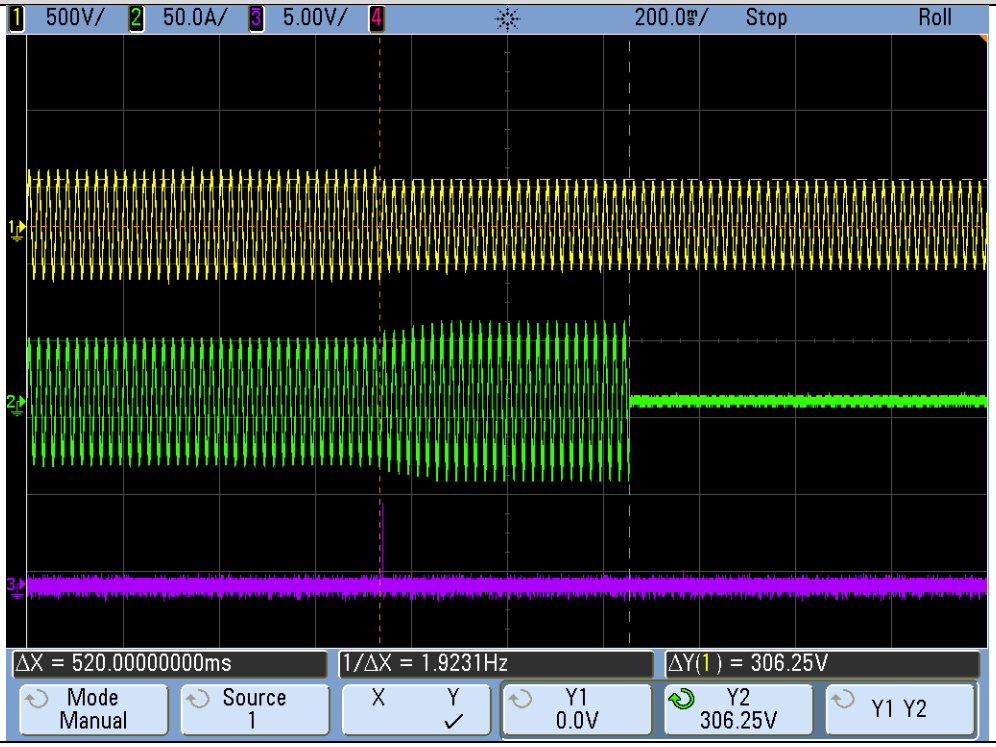
Under voltage, Stage 1 - Test 5



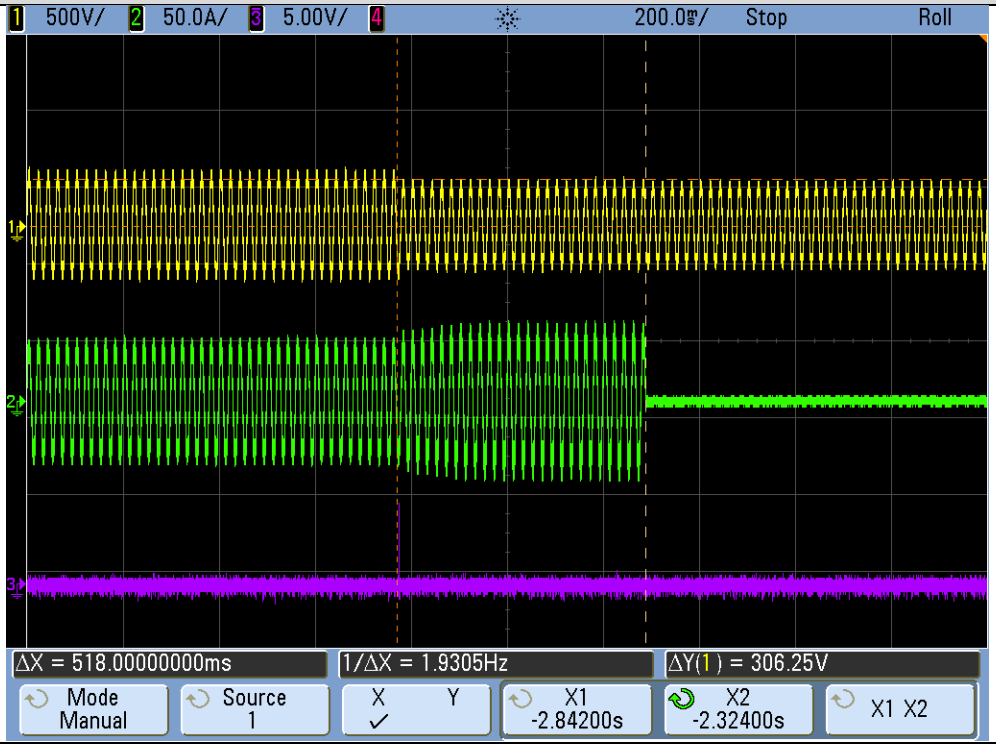
Under voltage, Stage 2 - Test 1



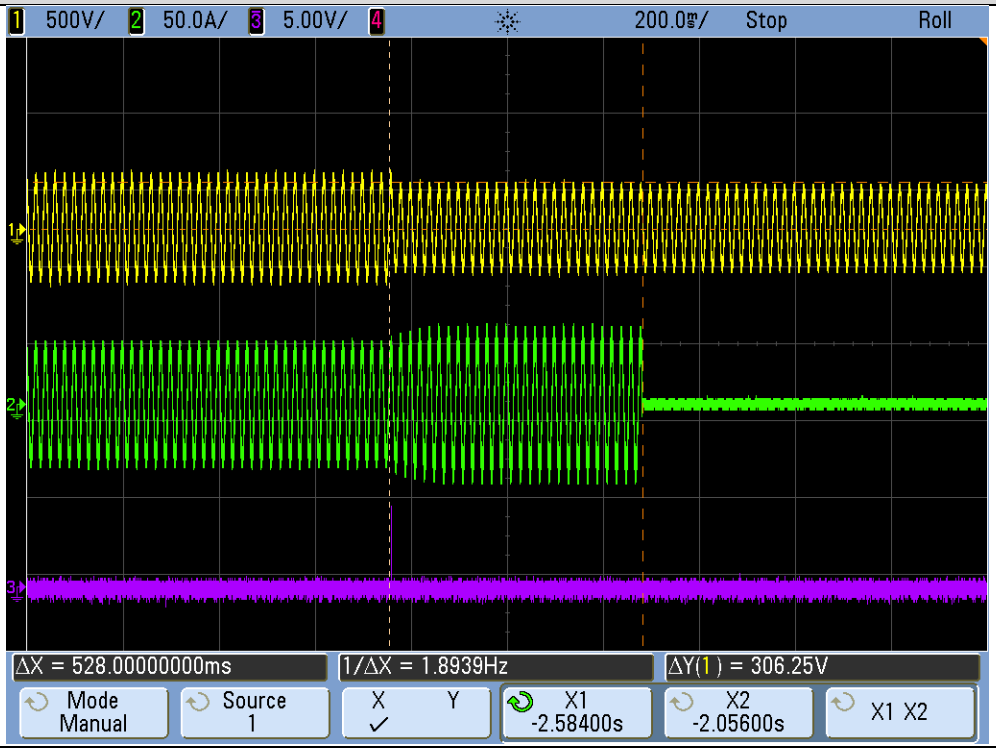
Under voltage, Stage 2 - Test 2



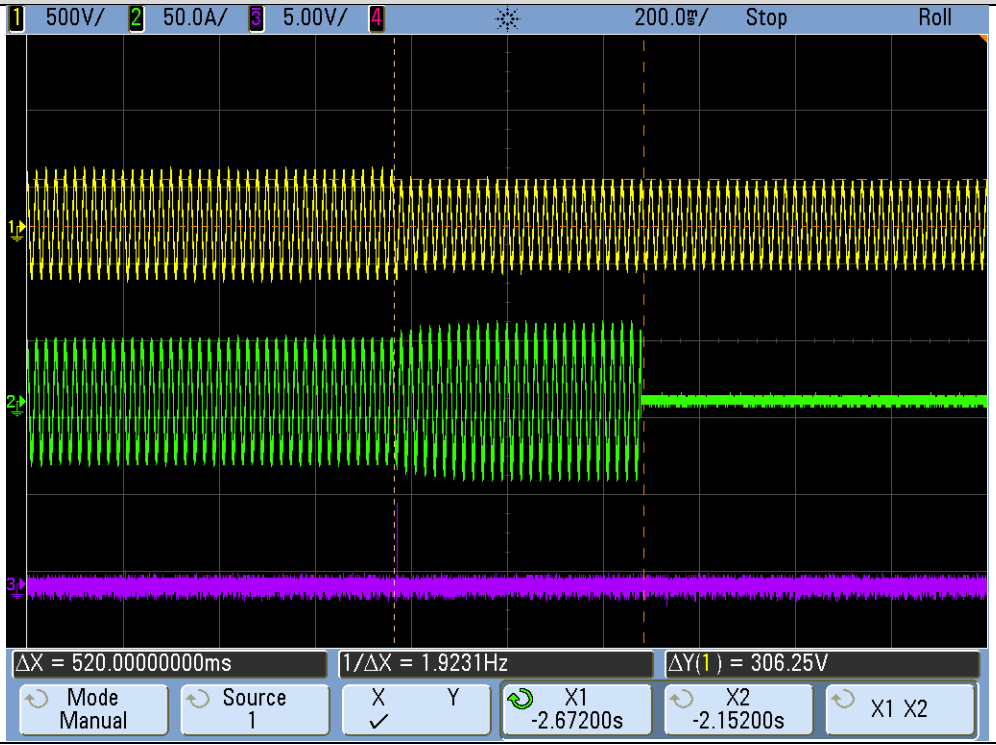
Under voltage, Stage 2 - Test 3



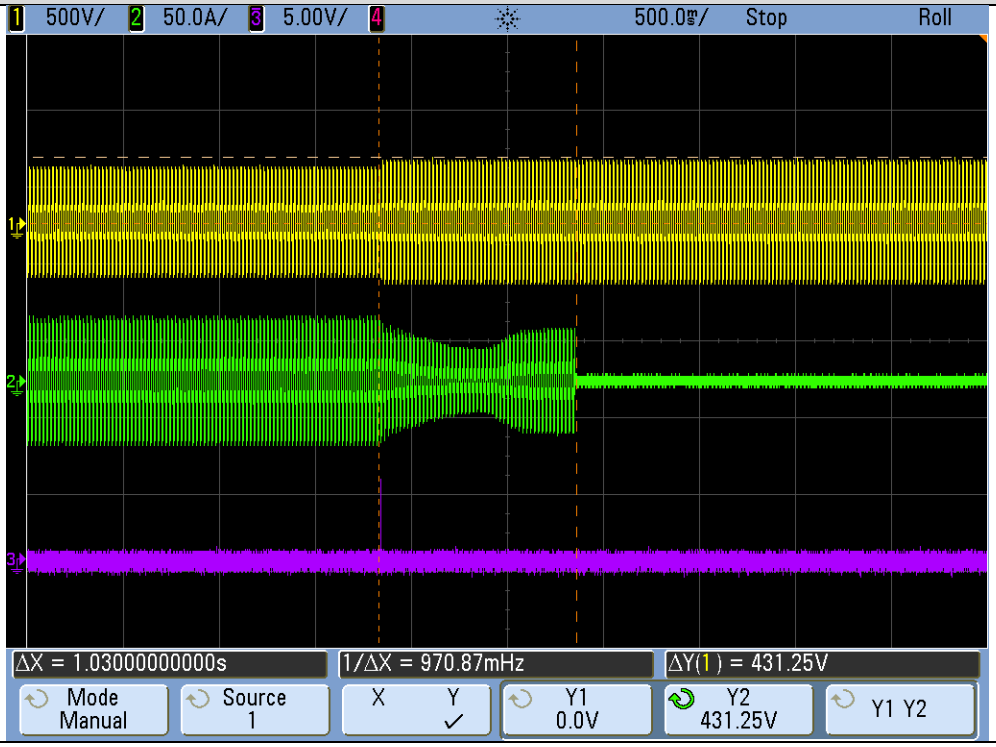
Under voltage, Stage 2 - Test 4



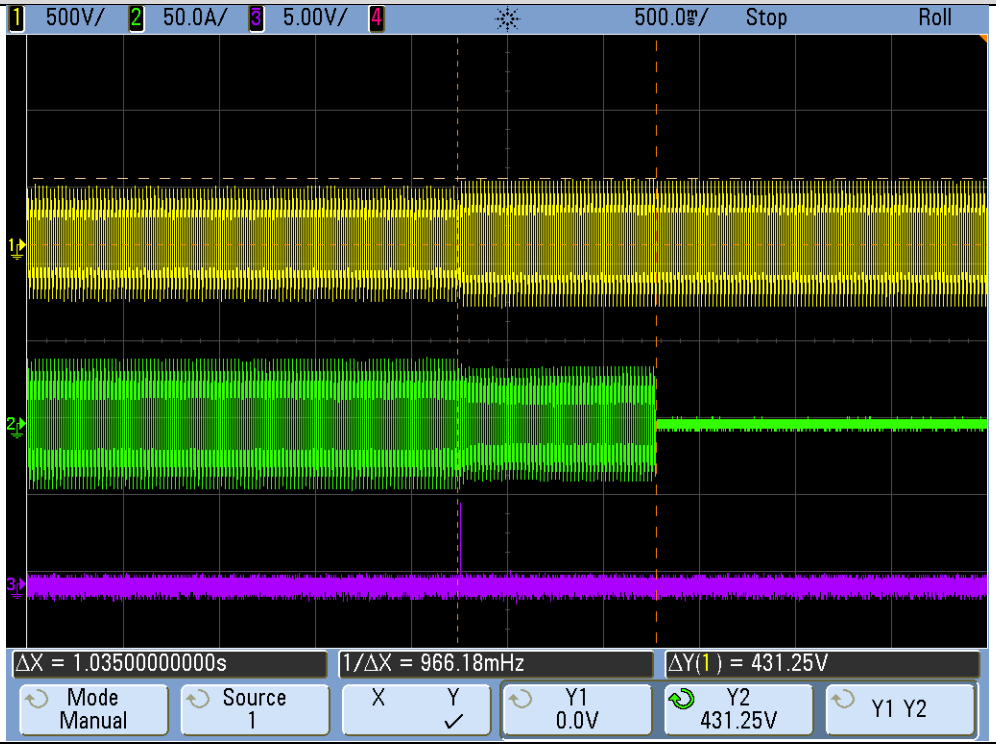
Under voltage, Stage 2 - Test 5



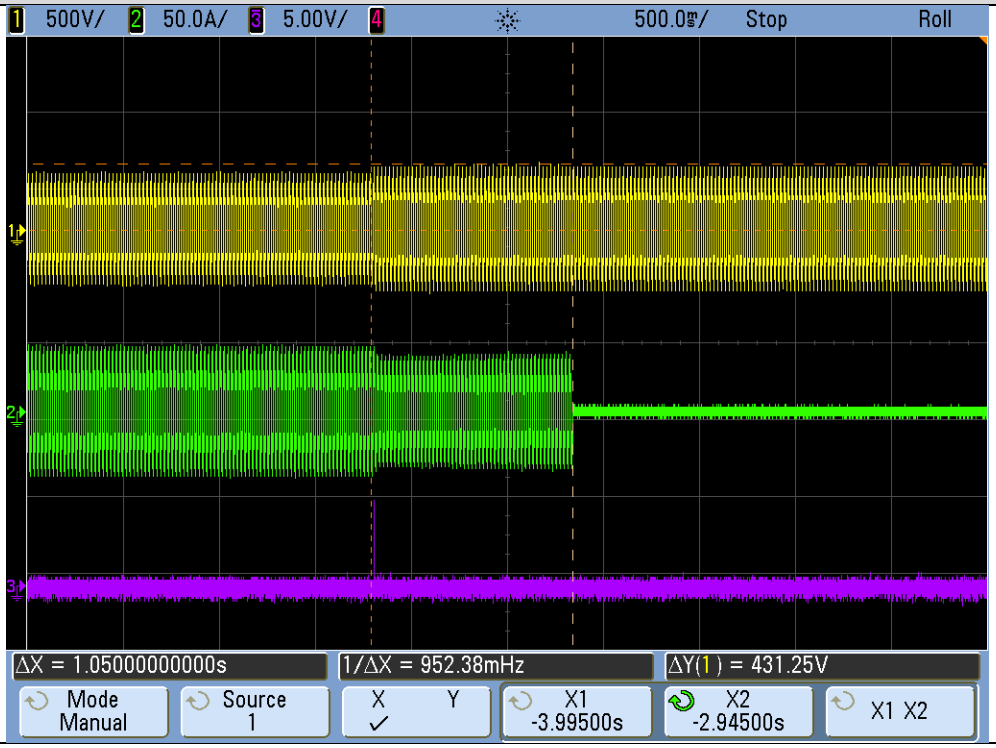
Over voltage, Stage 1 - Test 1



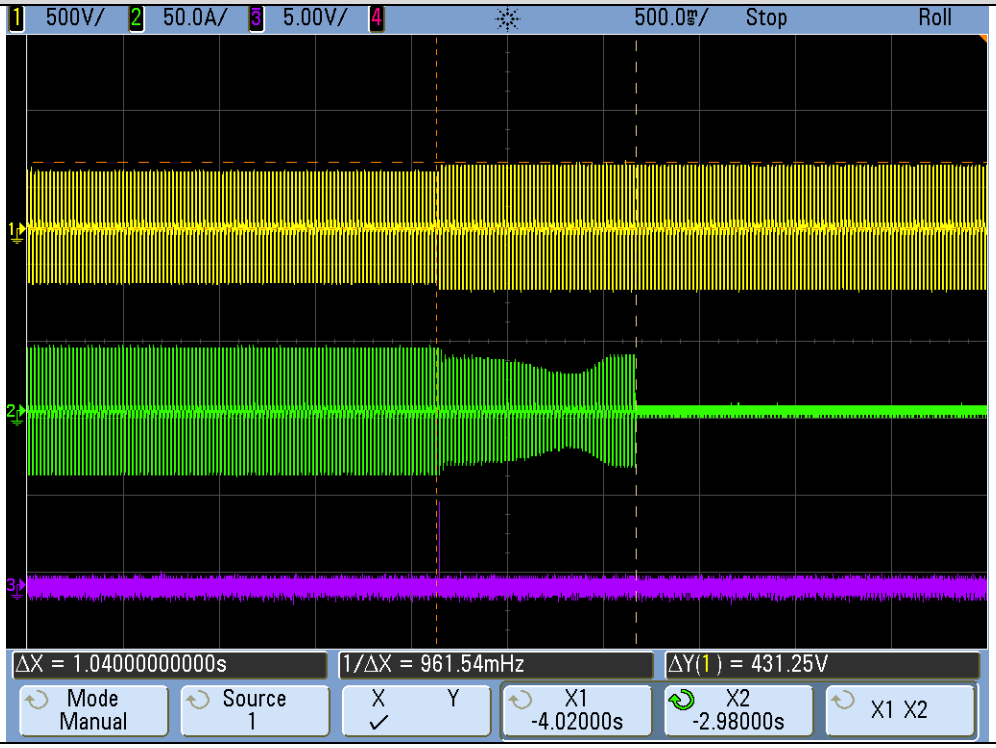
Over voltage, Stage 1 - Test 2



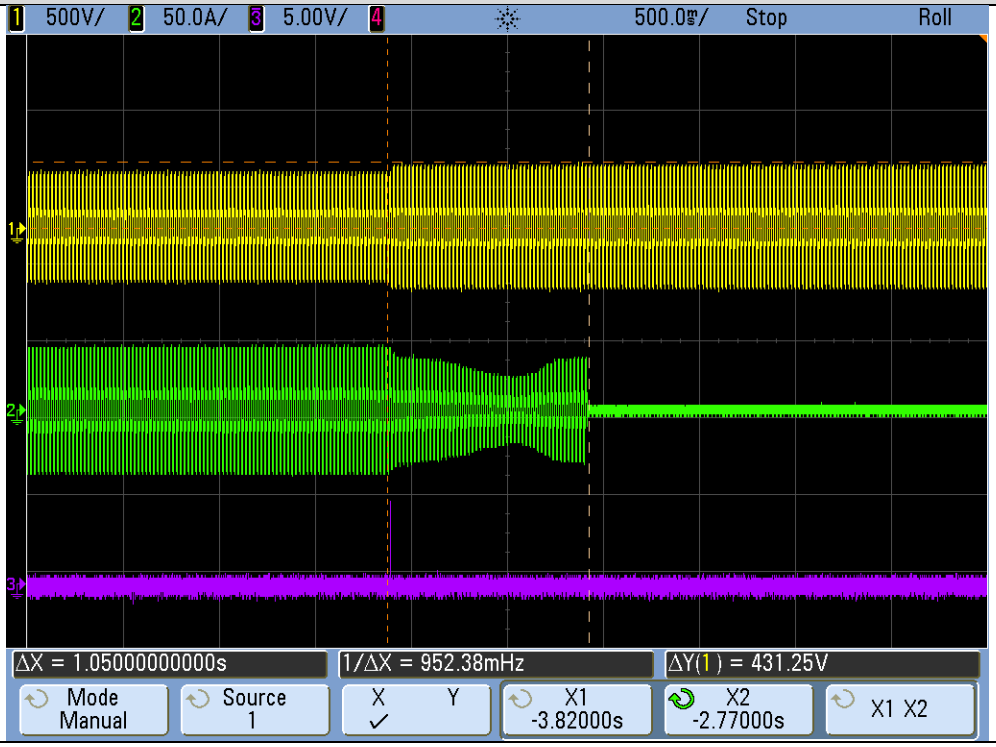
Over voltage, Stage 1 - Test 3



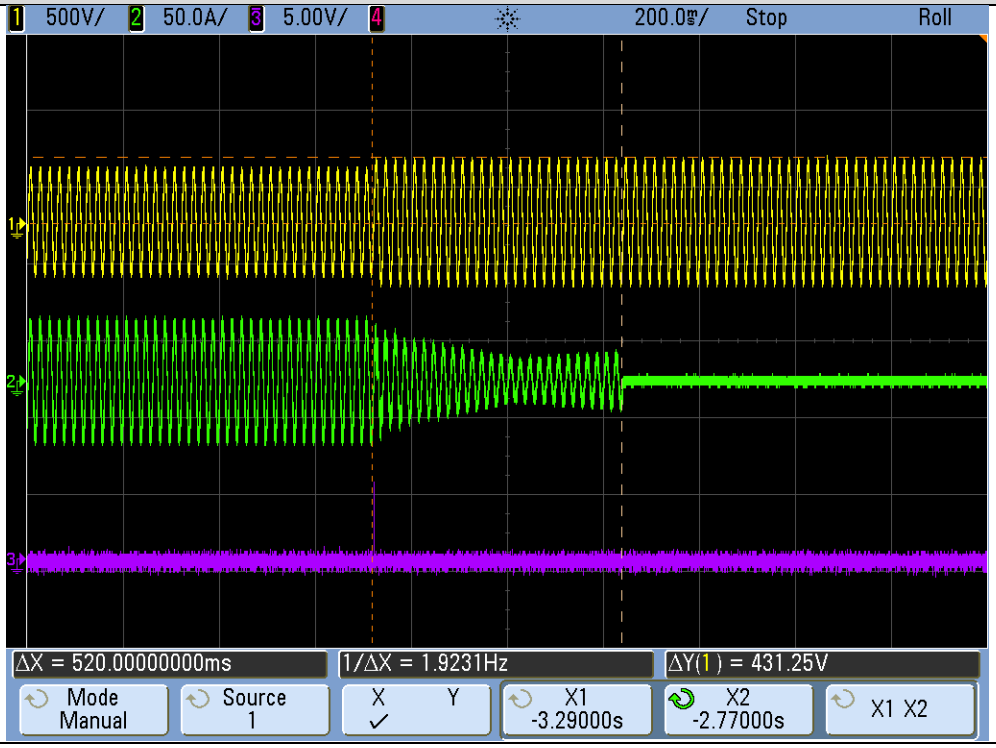
Over voltage, Stage 1 - Test 4



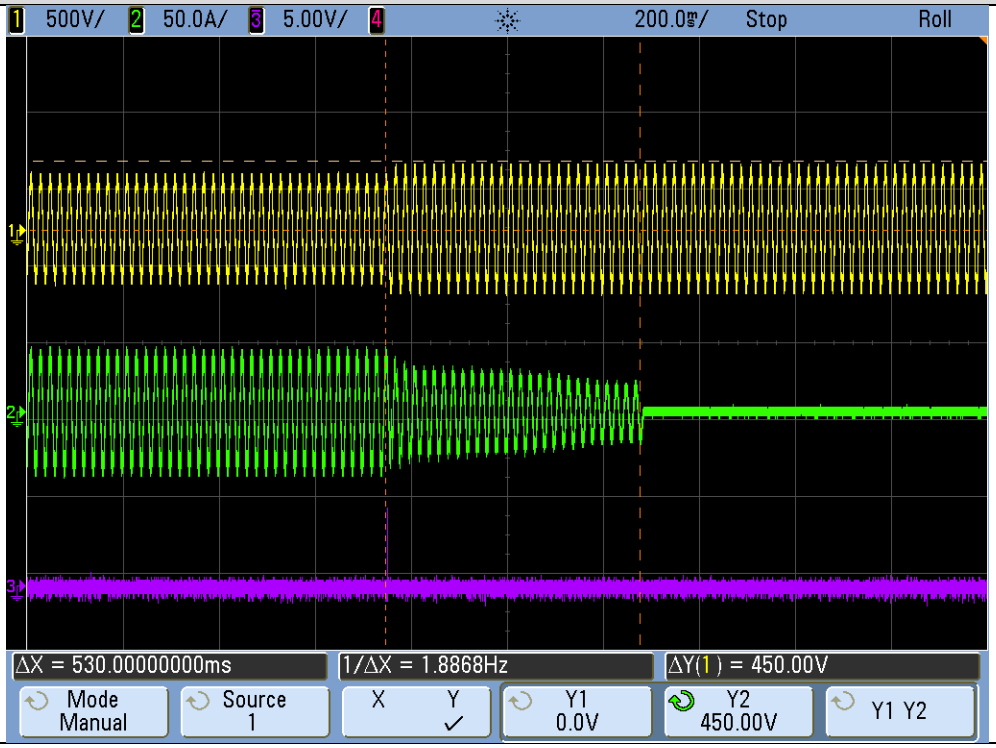
Over voltage, Stage 1 - Test 5



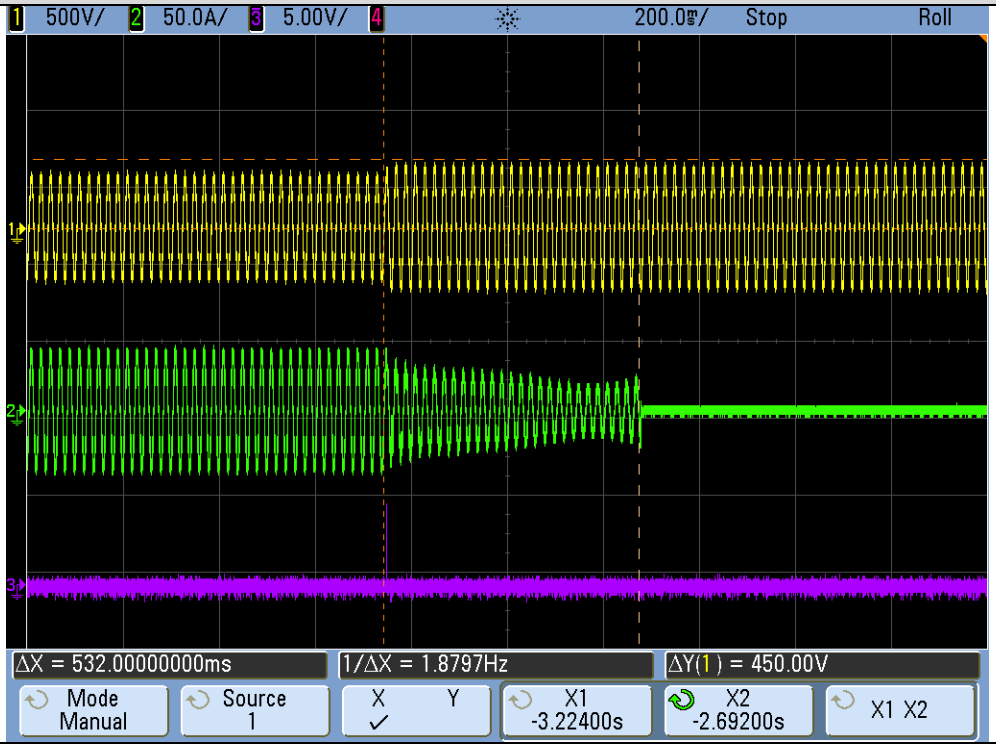
Over voltage, Stage 2 - Test 1



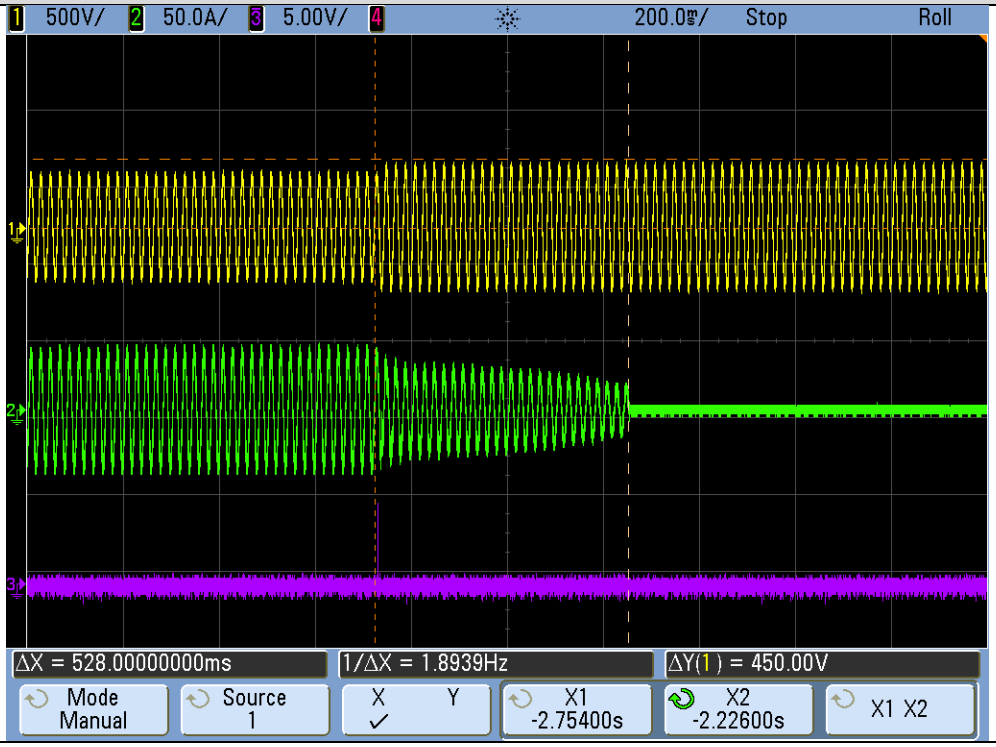
Over voltage, Stage 2 - Test 2



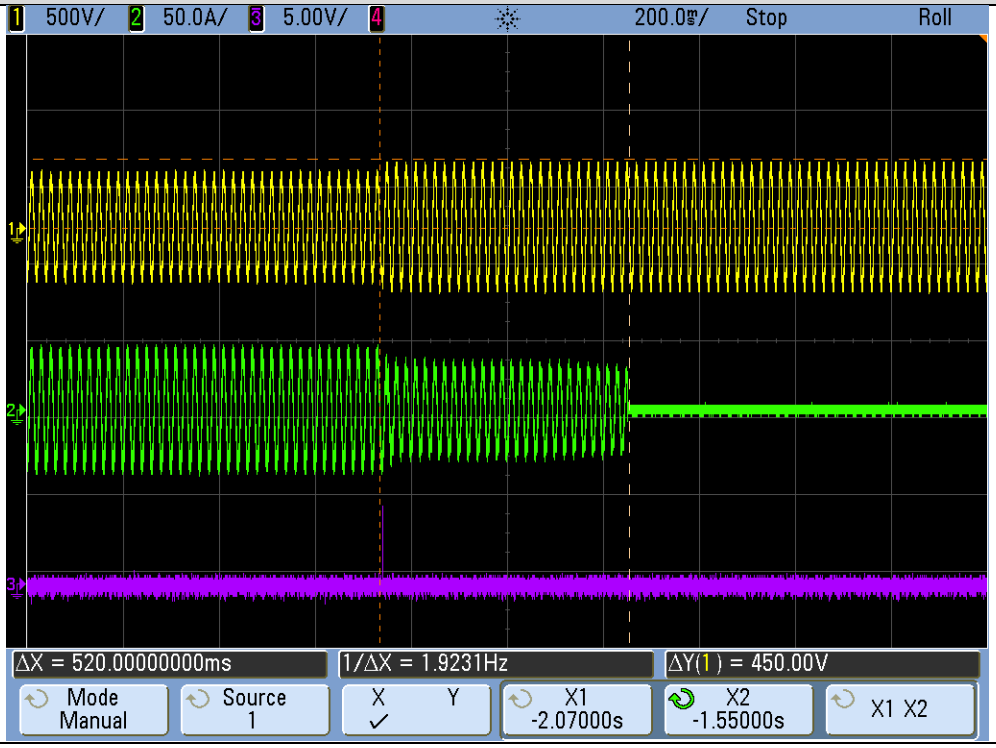
Over voltage, Stage 2 - Test 3



Over voltage, Stage 2 - Test 4



Over voltage, Stage 2 - Test 5



4.1.3 Over/ Under Frequency

4.1.3.1 Trip value test.

The tests have been done according to point 13.8.3.3 of the Standard.

It was followed the procedure below:

- For underfrequency protection: Starting from a frequency level 0.3 Hz above the trip value of the protection function to be tested, the frequency is decreased 0.05 Hz in steps of at least 150% of the trip time delay stated in the protection function to be tested.
- For overfrequency protection: Starting from a frequency level 0.3 Hz below the trip value of the protection function to be tested, the frequency is increased 0.05 Hz in steps of at least 150% of the trip time delay stated in the protection function to be tested.

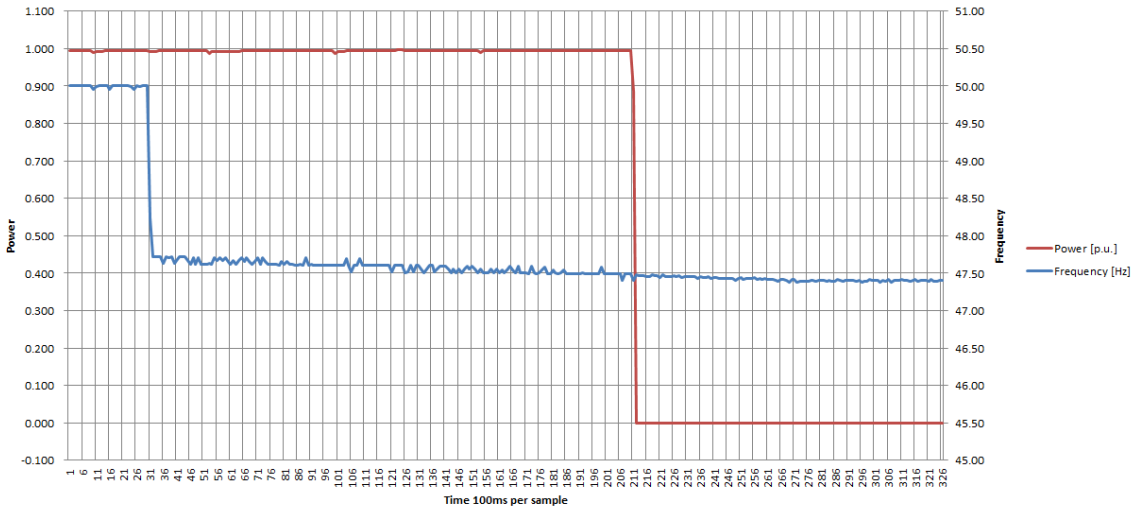
Maximum frequency deviation allowed is ±0.10 Hz. Each test was repeated five times.

Following tables show the test results.

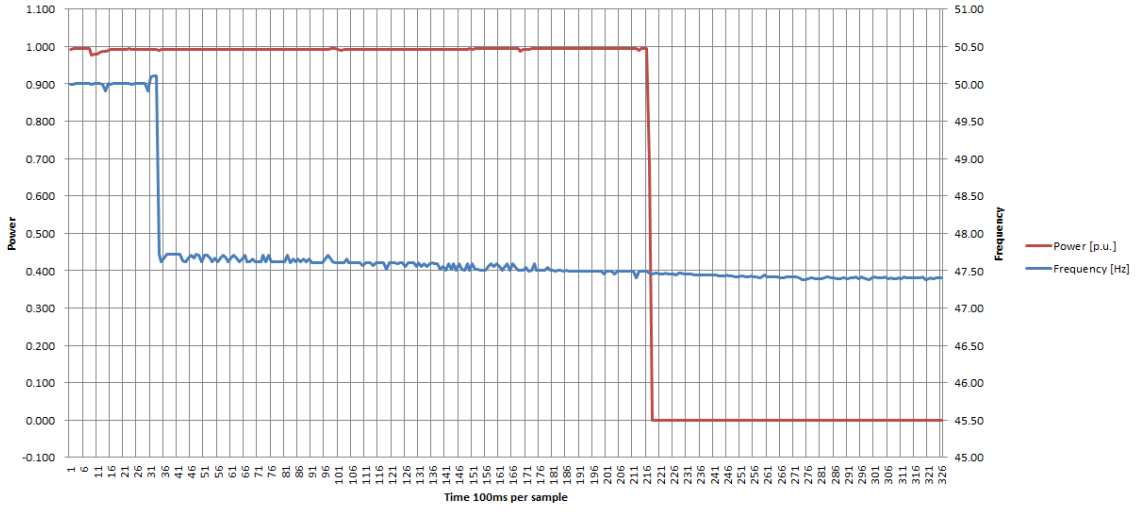
Stage/Prot Function	Test	Frequency at the start (Hz)	Trip Frequency Desired (Hz)	Trip frequency measured (Hz)	Disconnection	Maximum deviation measured (Hz)
U/F st1 47.5 Hz	1	50	47.50	47.47	☐ NO ☒ YES	-0.03
	2	50	47.50	47.45	☐ NO ☒ YES	-0.05
	3	50	47.50	47.47	☐ NO ☒ YES	-0.03
	4	50	47.50	47.47	☐ NO ☒ YES	-0.03
	5	50	47.50	47.48	☐ NO ☒ YES	-0.02
U/f st2 47.0 Hz	1	50	47.00	46.93	☐ NO ☒ YES	-0.07
	2	50	47.00	46.94	☐ NO ☒ YES	-0.06
	3	50	47.00	46.94	☐ NO ☒ YES	-0.06
	4	50	47.00	46.95	☐ NO ☒ YES	-0.05
	5	50	47.00	46.93	☐ NO ☒ YES	-0.07
O/F st1 51.5 Hz	1	50	51.50	51.51	☐ NO ☒ YES	0.01
	2	50	51.50	51.50	☐ NO ☒ YES	0.00
	3	50	51.50	51.51	☐ NO ☒ YES	0.01
	4	50	51.50	51.49	☐ NO ☒ YES	-0.01
	5	50	51.50	51.50	☐ NO ☒ YES	0.00
O/F st2 52.0 Hz	1	50	52.00	52.06	☐ NO ☒ YES	0.06
	2	50	52.00	52.06	☐ NO ☒ YES	0.06
	3	50	52.00	52.07	☐ NO ☒ YES	0.07
	4	50	52.00	52.08	☐ NO ☒ YES	0.08
	5	50	52.00	52.08	☐ NO ☒ YES	0.08

Test results are graphically shown in following pages.

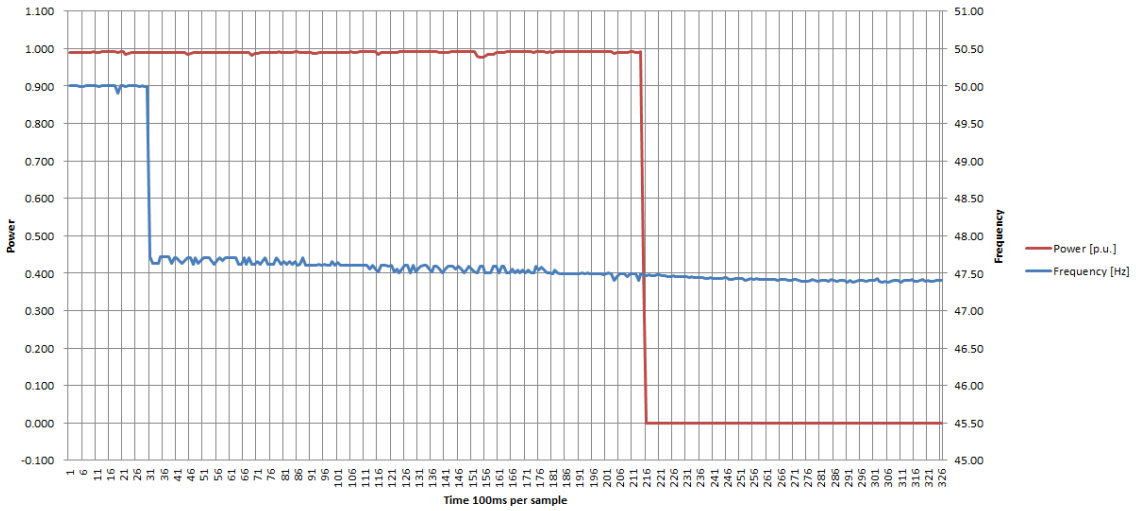
Under frequency, Stage 1 - Test 1



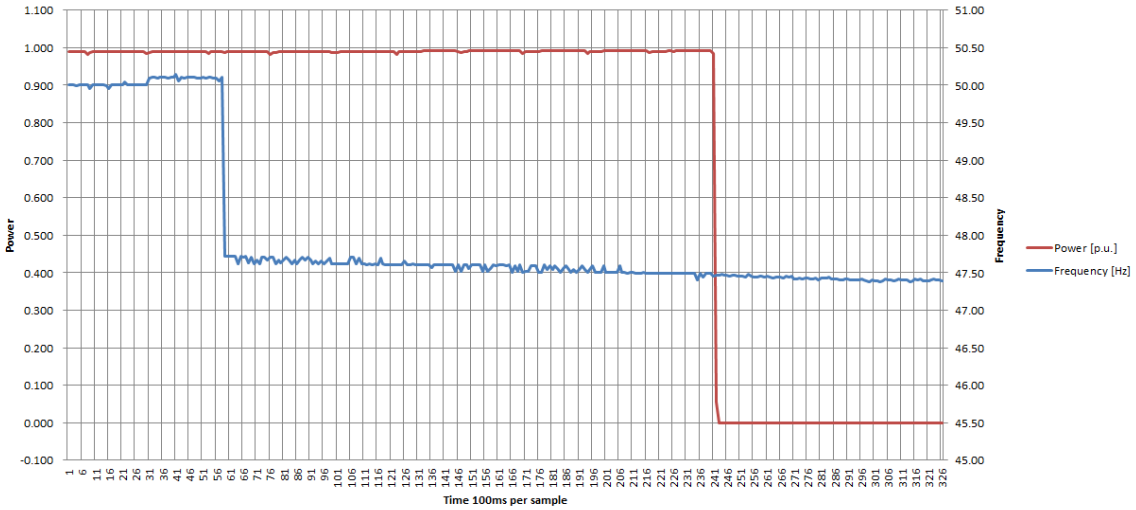
Under frequency, Stage 1 - Test 2



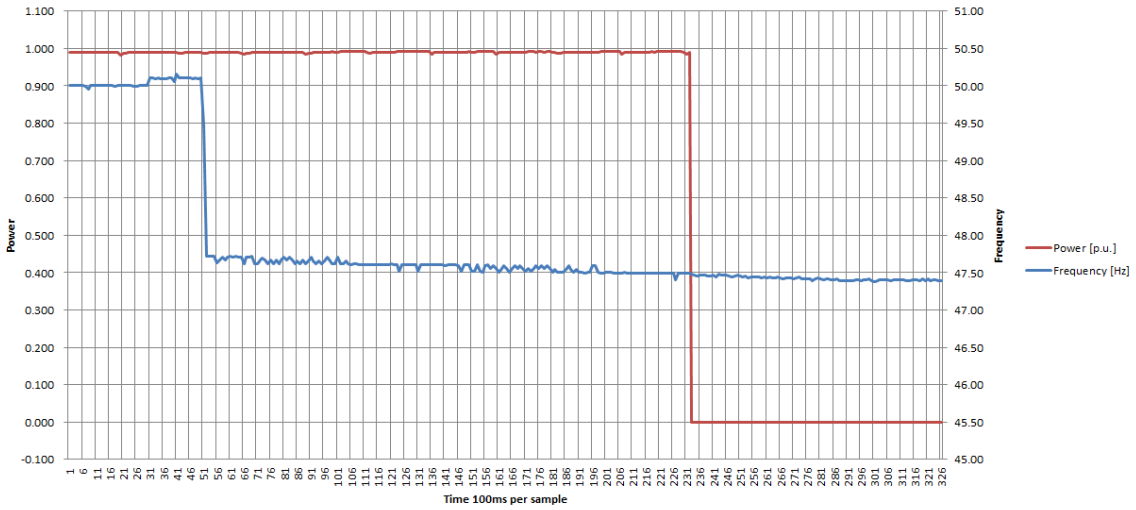
Under frequency, Stage 1 - Test 3



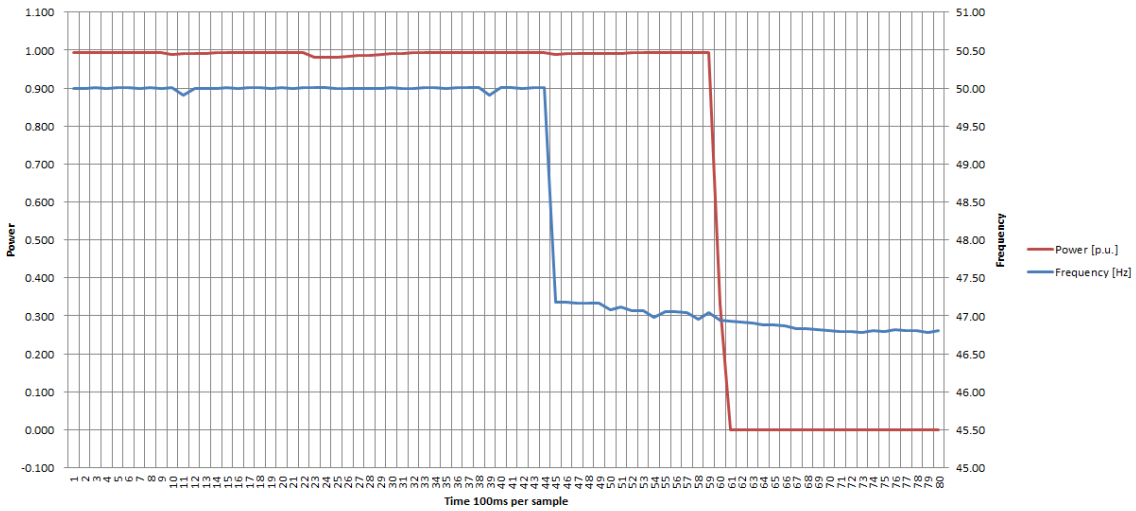
Under frequency, Stage 1 - Test 4



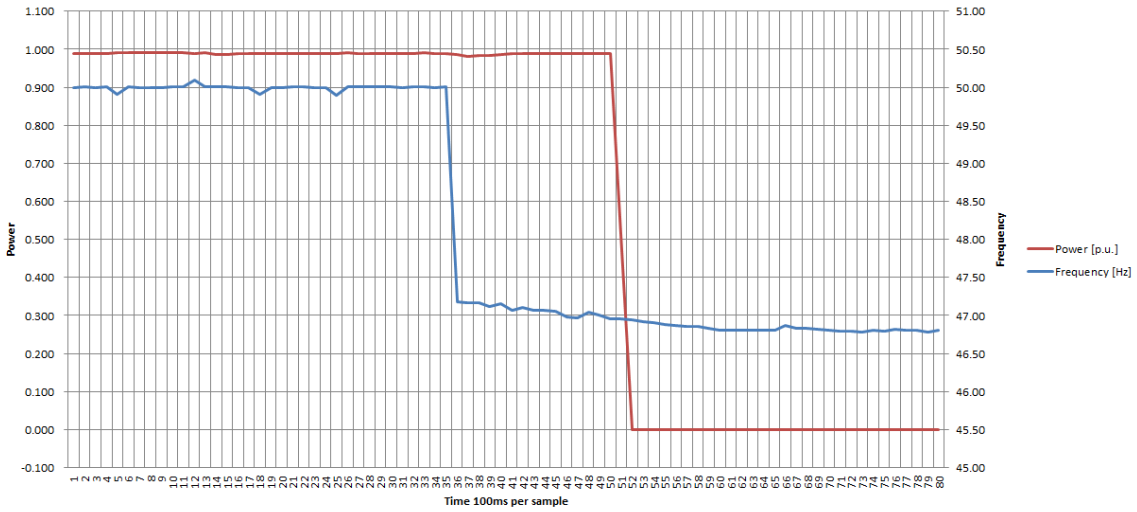
Under frequency, Stage 1 - Test 5



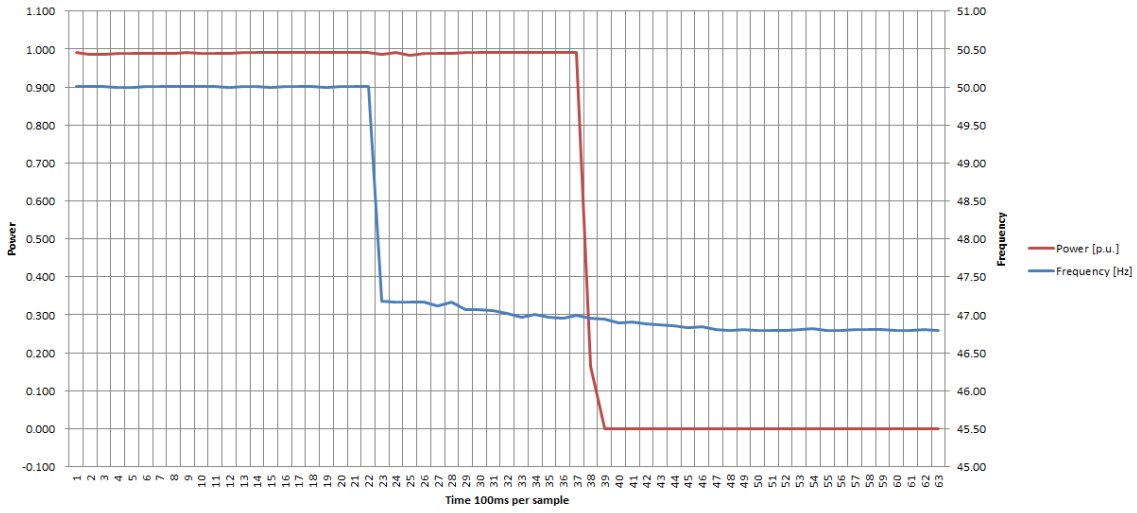
Under frequency, Stage 2 - Test 1



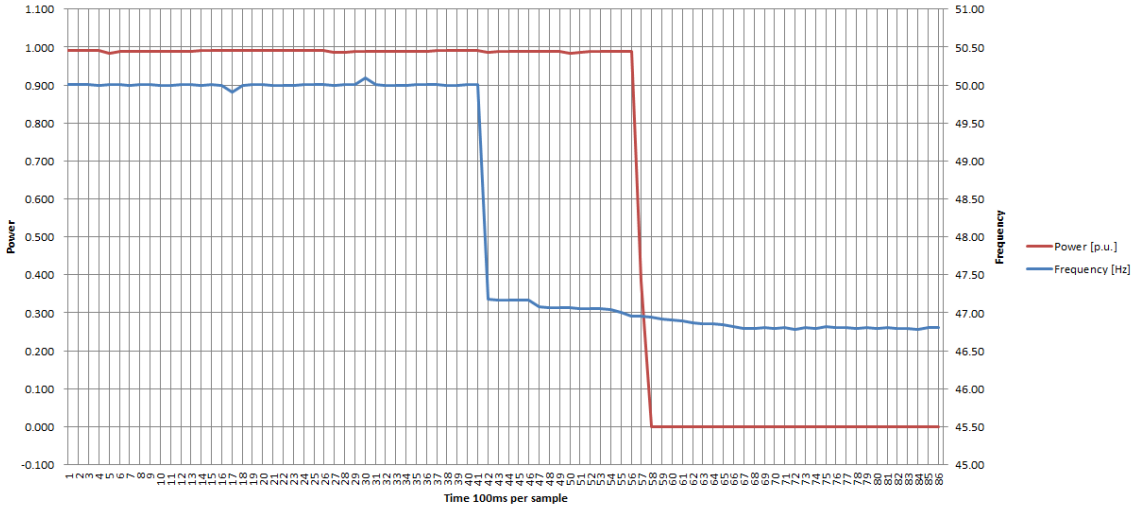
Under frequency, Stage 2 - Test 2



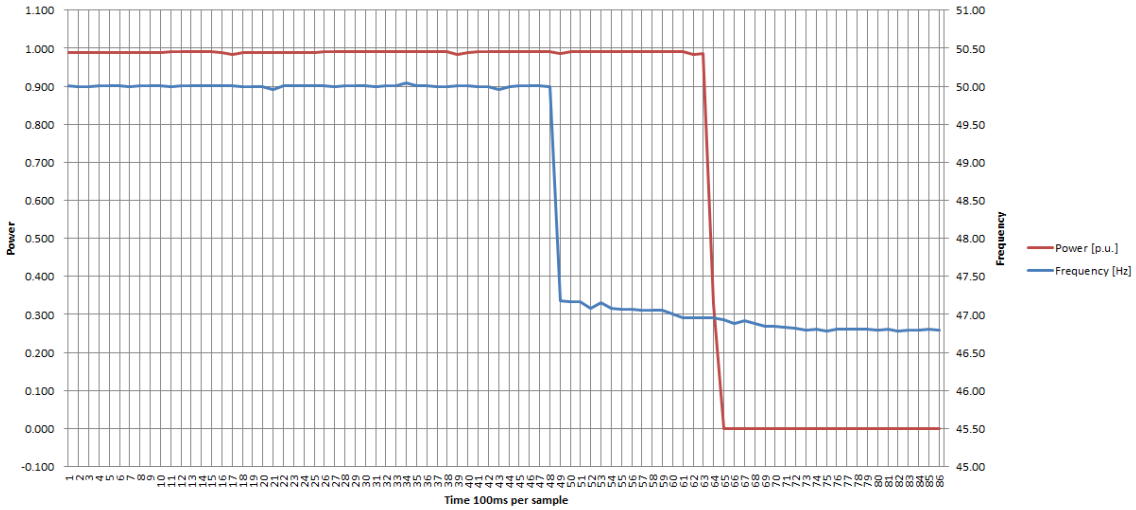
Under frequency, Stage 2 - Test 3



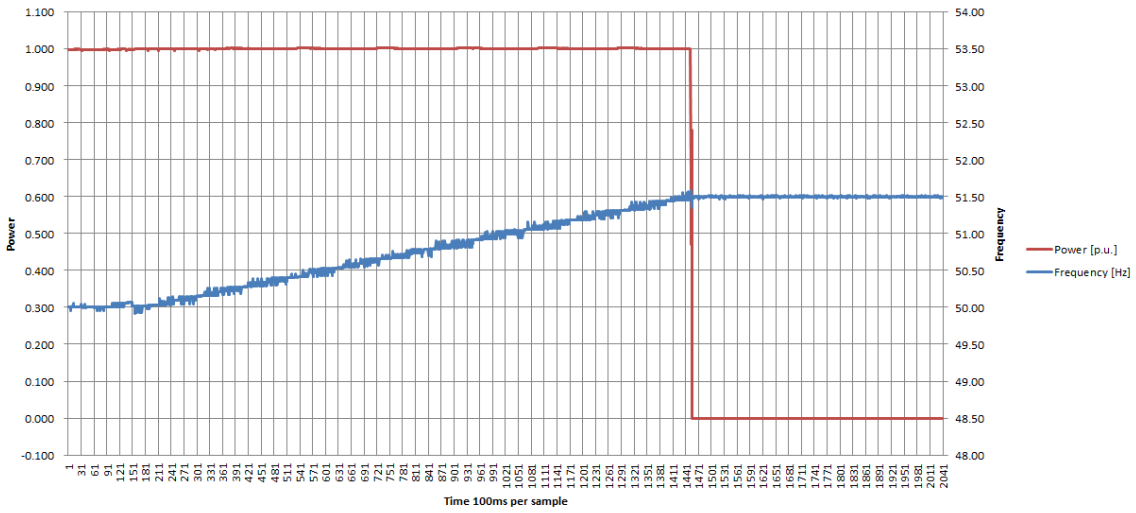
Under frequency, Stage 2 - Test 4



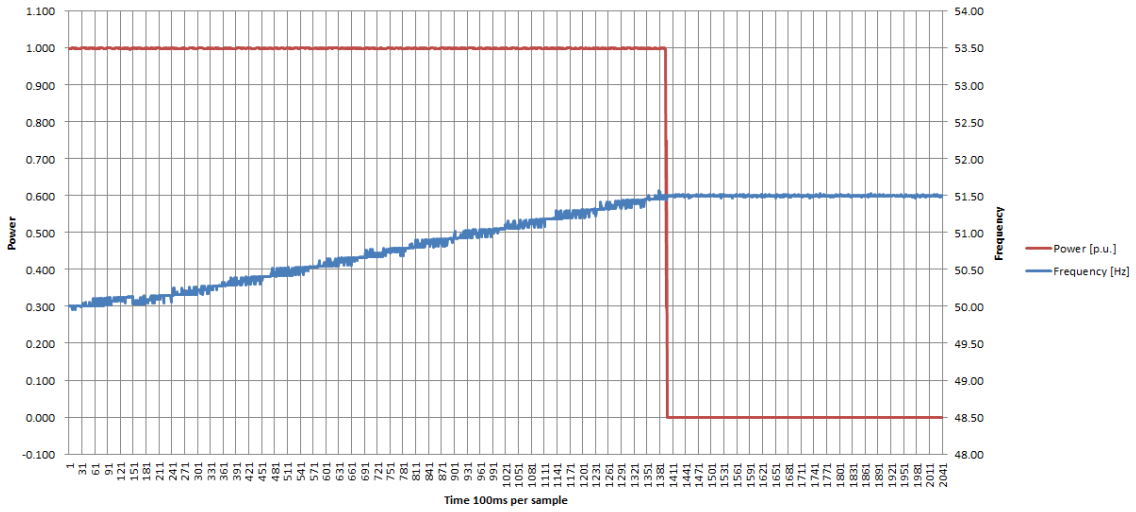
Under frequency, Stage 2 - Test 5



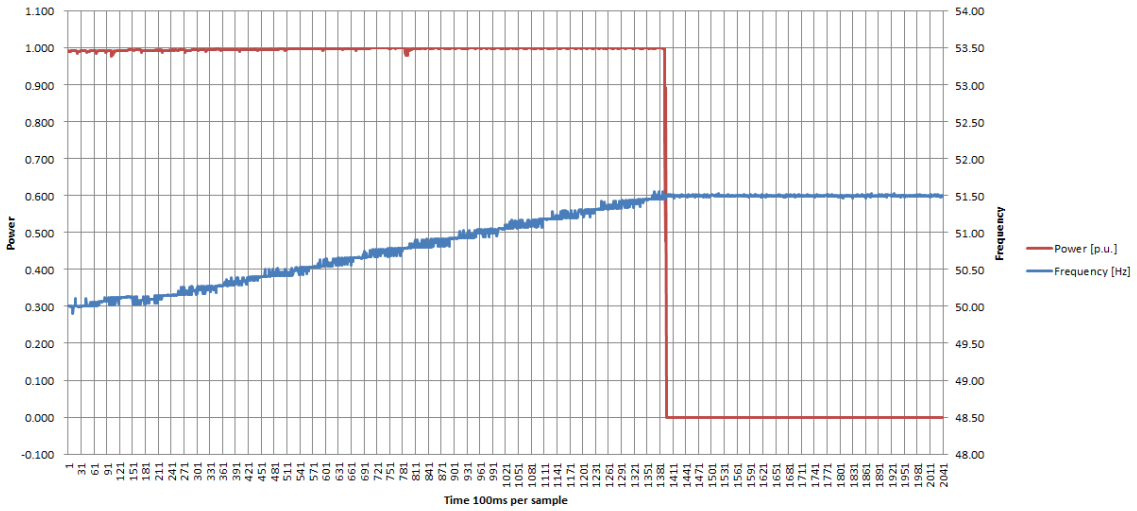
Over frequency, Stage 1 - Test 1



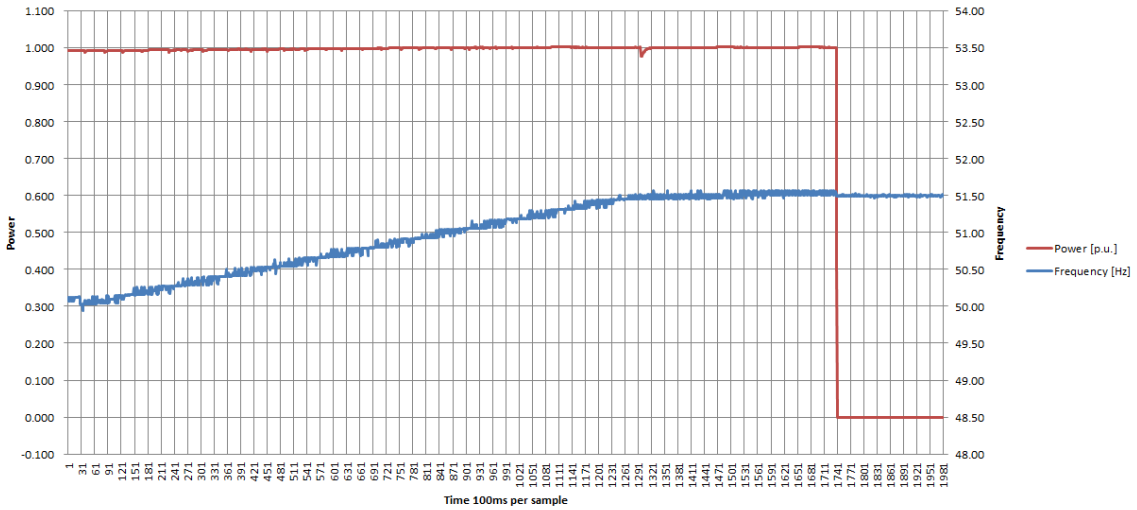
Over frequency, Stage 1 - Test 2



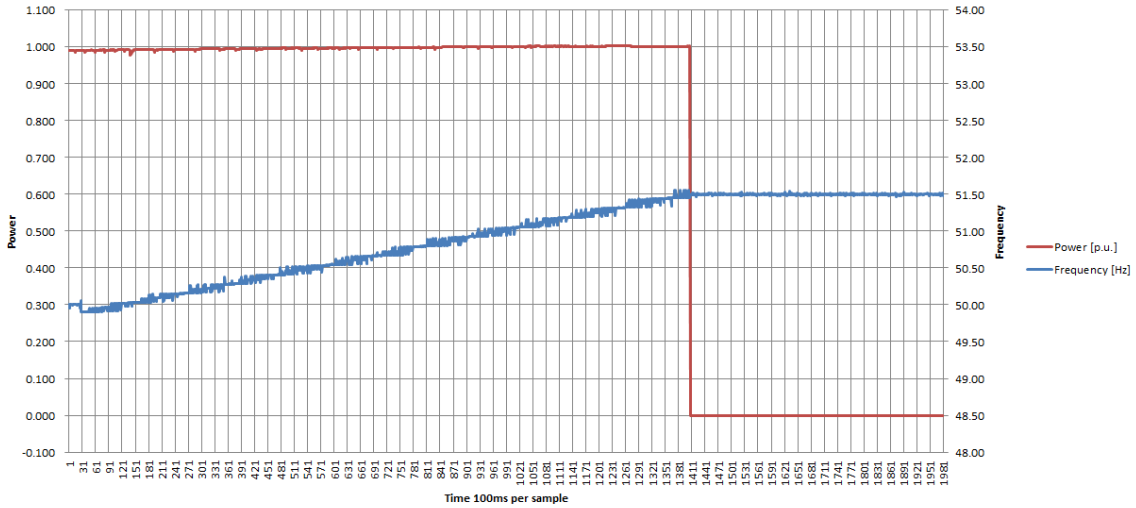
Over frequency, Stage 1 - Test 3



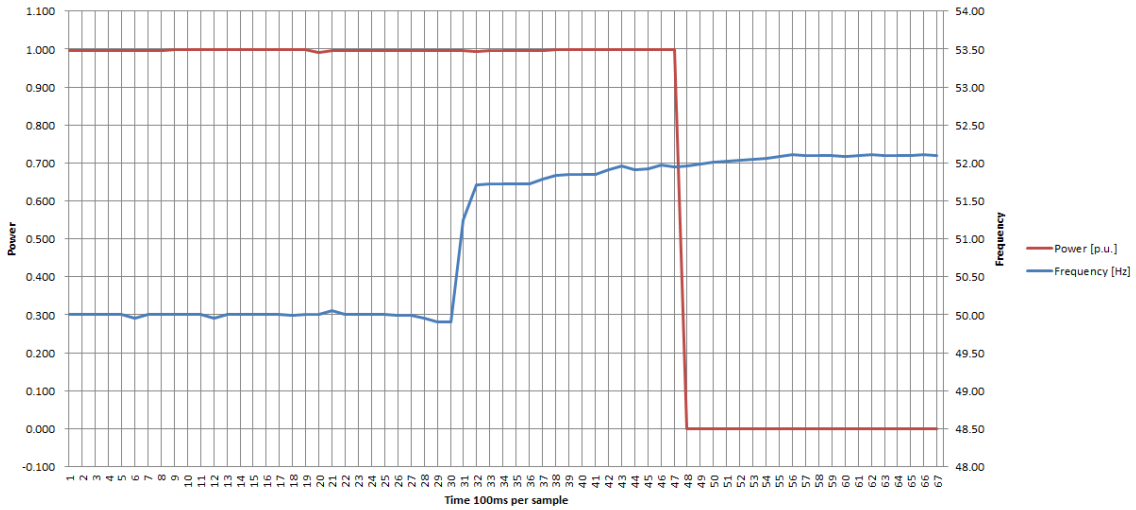
Over frequency, Stage 1 - Test 4



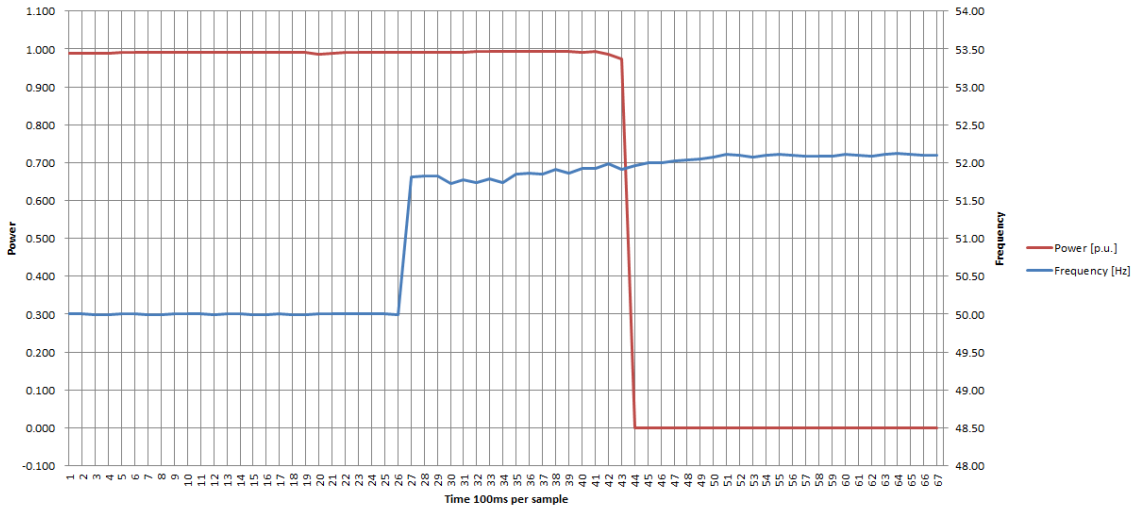
Over frequency, Stage 1 - Test 5



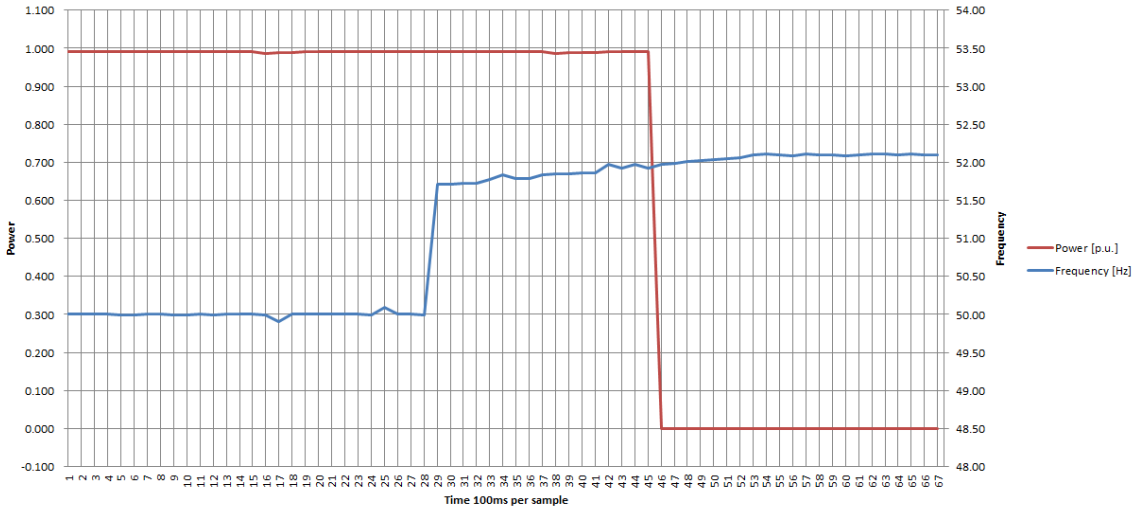
Over frequency, Stage 2 - Test 1



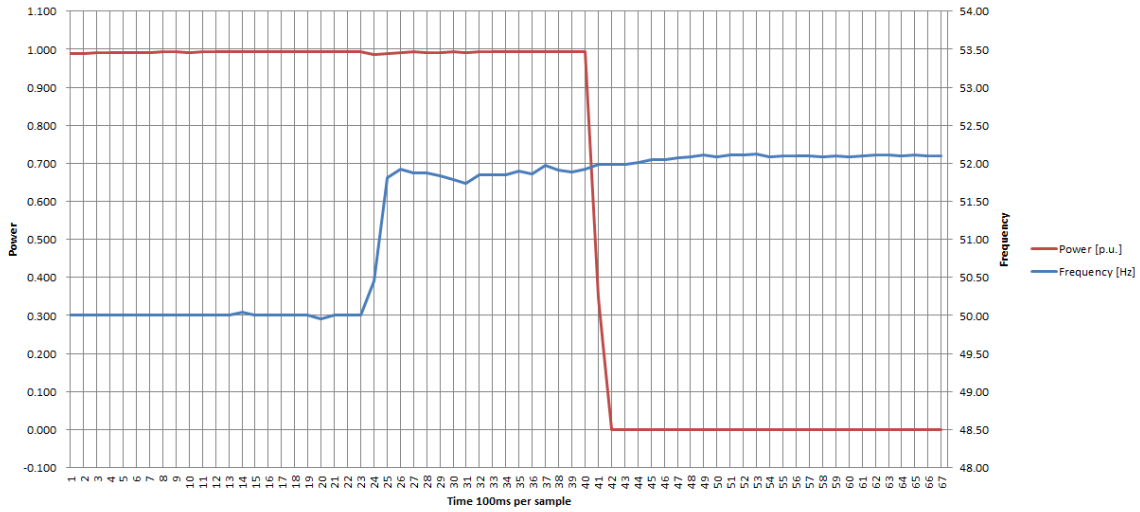
Over frequency, Stage 2 - Test 2



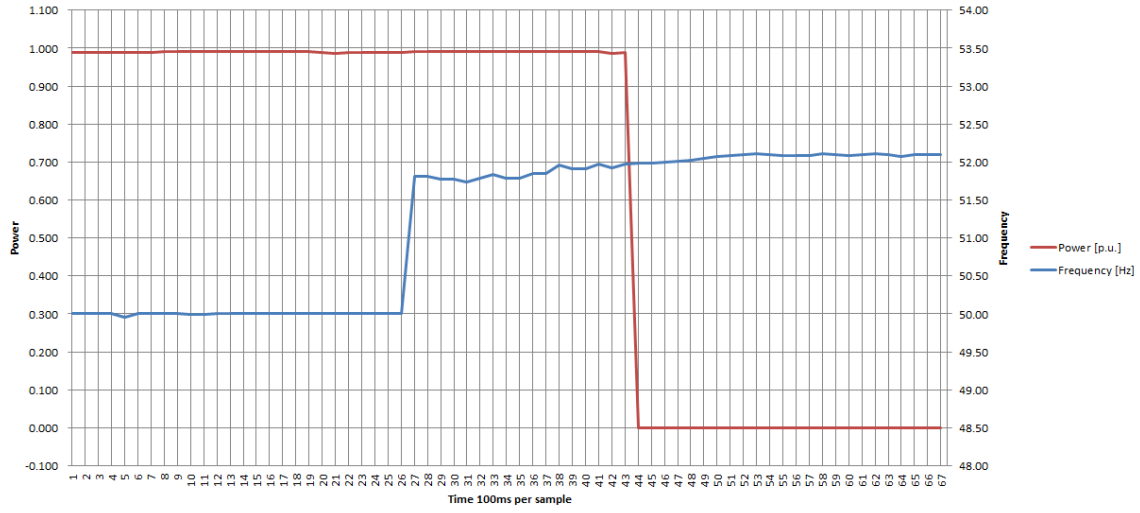
Over frequency, Stage 2 - Test 3



Over frequency, Stage 2 - Test 4



Over frequency, Stage 2 - Test 5



4.1.3.2 Trip time test.

The tests have been made as the following procedure:

- For underfrequency protection: Starting from a frequency level above the trip value of the protection function to be tested, the frequency is decreased in a step to a value below the frequency setpoint of the protection function and it´s measured from that instant the time it takes to disconnect.
- For overfrequency protection: Starting from a frequency level below the trip value of the protection function to be tested, the frequency is increased in a step to a value above the frequency setpoint of the protection function and it´s measured from that instant the time it takes to disconnect.

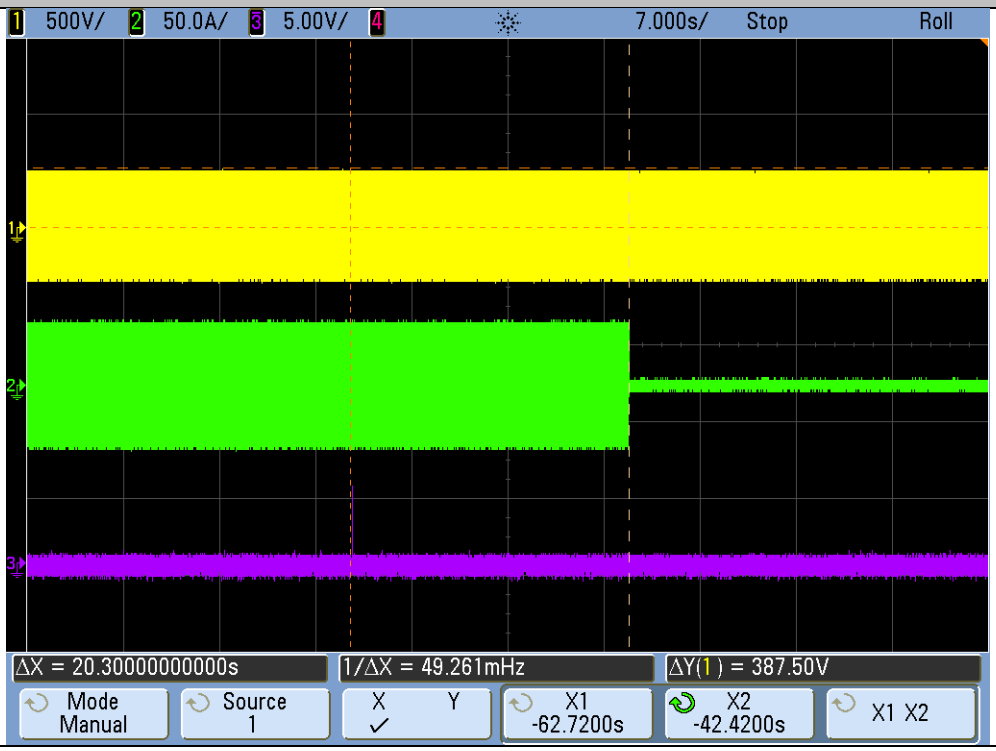
The tests have been performed at rated power. Each protection function has been tested 5 times.

Following tables show the test results.

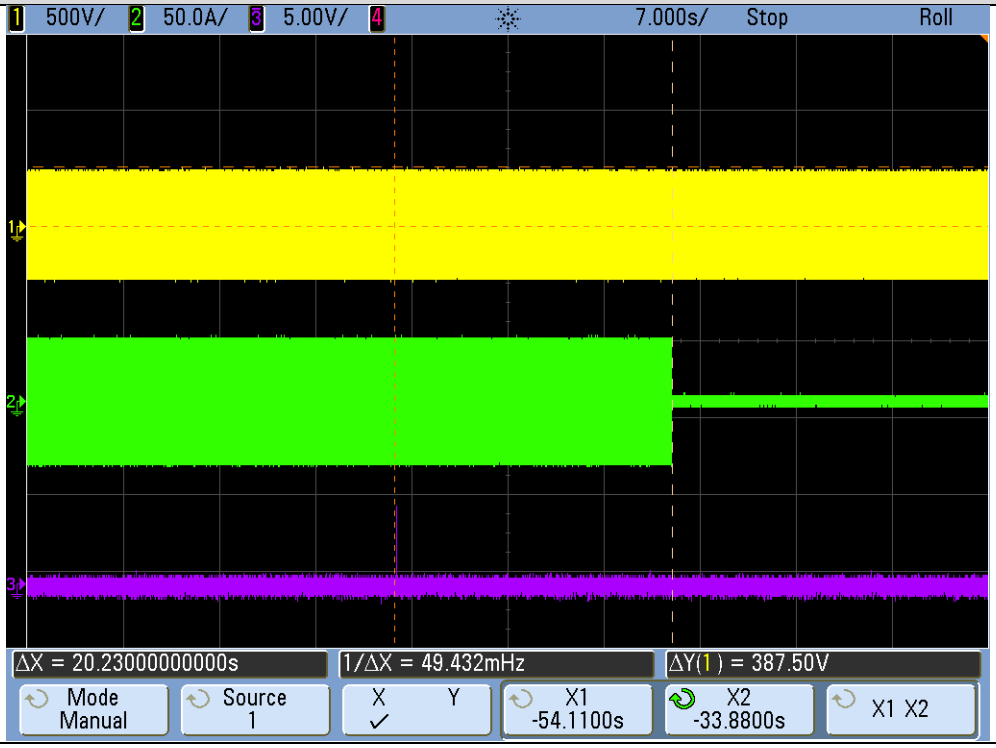
Stage/Prot Function	Test	Delay Time limit (s)	Maximum trip time (s)	Trip time measured (s)	Disconnection
U/F st1 47.5 Hz	1	20	20.5	20.300	☐ NO ☒ YES
	2	20	20.5	20.230	☐ NO ☒ YES
	3	20	20.5	20.300	☐ NO ☒ YES
	4	20	20.5	20.370	☐ NO ☒ YES
	5	20	20.5	20.300	☐ NO ☒ YES
U/f st2 47.0 Hz	1	0.5	1.0	0.646	☐ NO ☒ YES
	2	0.5	1.0	0.669	☐ NO ☒ YES
	3	0.5	1.0	0.657	☐ NO ☒ YES
	4	0.5	1.0	0.660	☐ NO ☒ YES
	5	0.5	1.0	0.648	☐ NO ☒ YES
O/F st1 51.5 Hz	1	90	90.5	90.300	☐ NO ☒ YES
	2	90	90.5	90.320	☐ NO ☒ YES
	3	90	90.5	90.360	☐ NO ☒ YES
	4	90	90.5	90.370	☐ NO ☒ YES
	5	90	90.5	90.306	☐ NO ☒ YES
O/F st2 52.0 Hz	1	0.5	1.0	0.516	☐ NO ☒ YES
	2	0.5	1.0	0.536	☐ NO ☒ YES
	3	0.5	1.0	0.544	☐ NO ☒ YES
	4	0.5	1.0	0.532	☐ NO ☒ YES
	5	0.5	1.0	0.516	☐ NO ☒ YES

Test results are graphically shown in following pages.

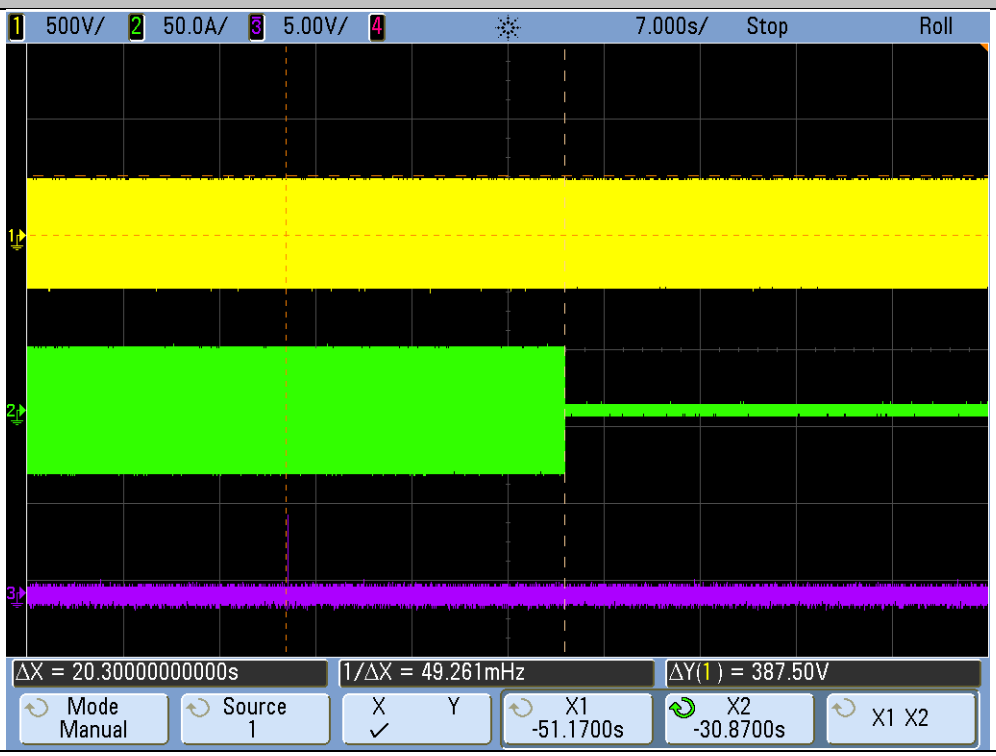
Under frequency, Stage 1 - Test 1



Under frequency, Stage 1 - Test 2

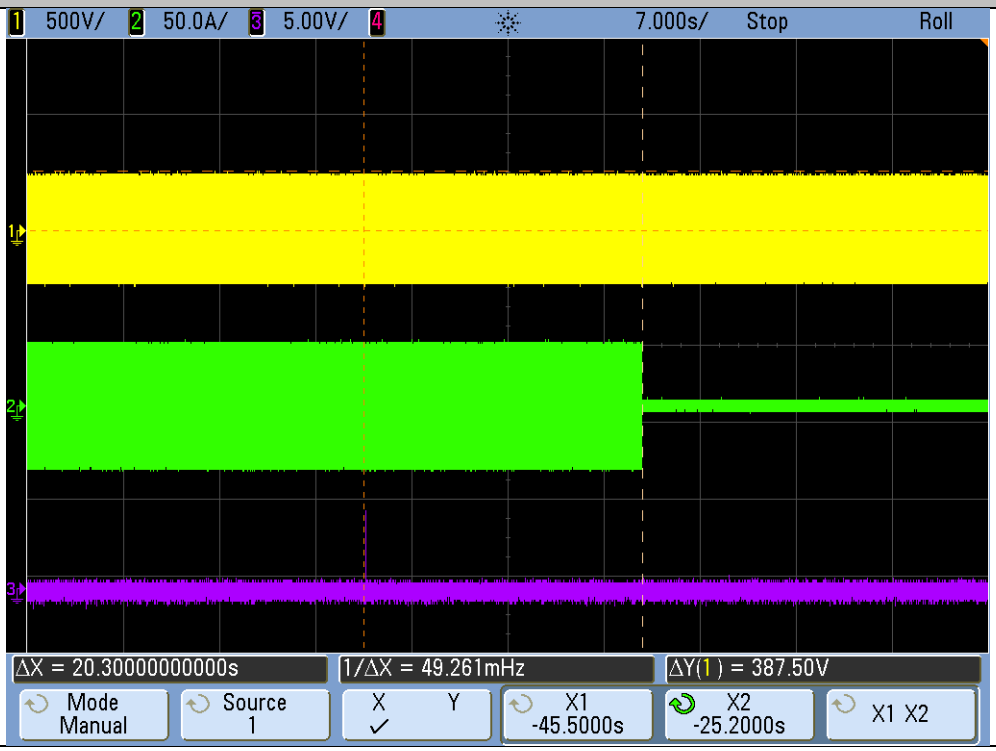


Under frequency, Stage 1 - Test 3

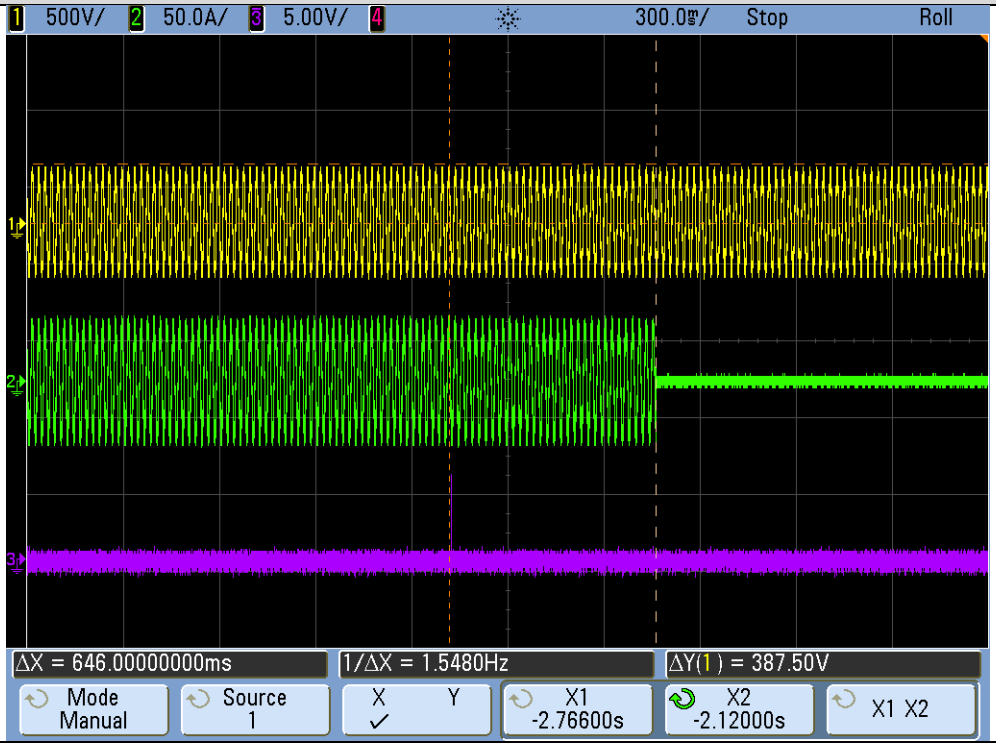


Under frequency, Stage 1 - Test 4

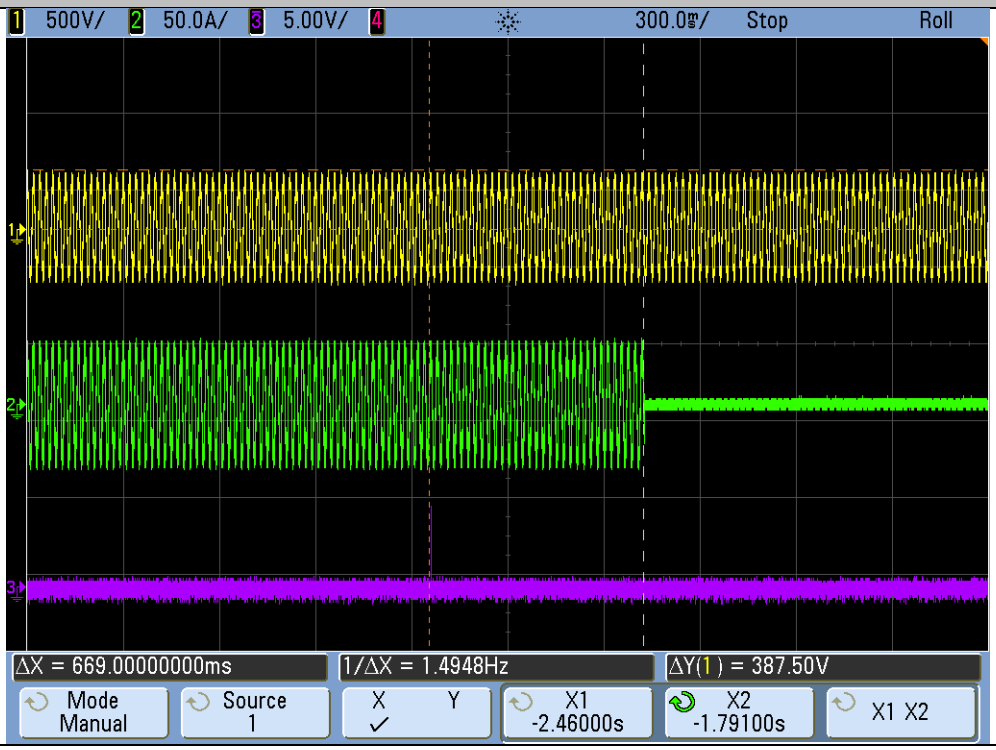
Under frequency, Stage 1 - Test 5



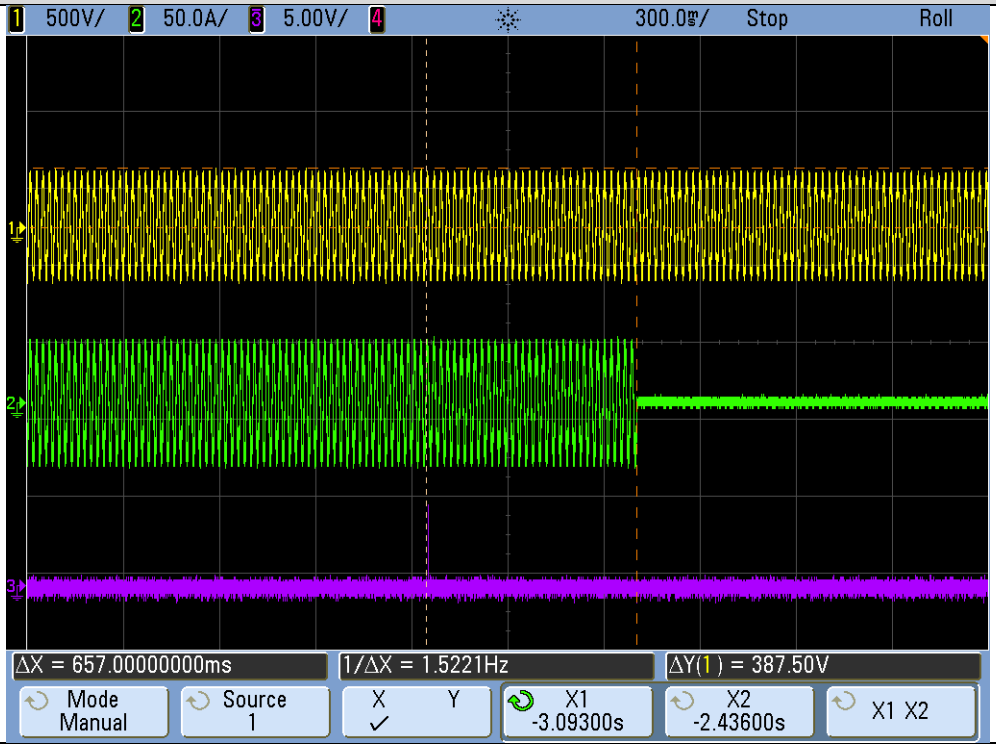
Under frequency, Stage 2 - Test 1



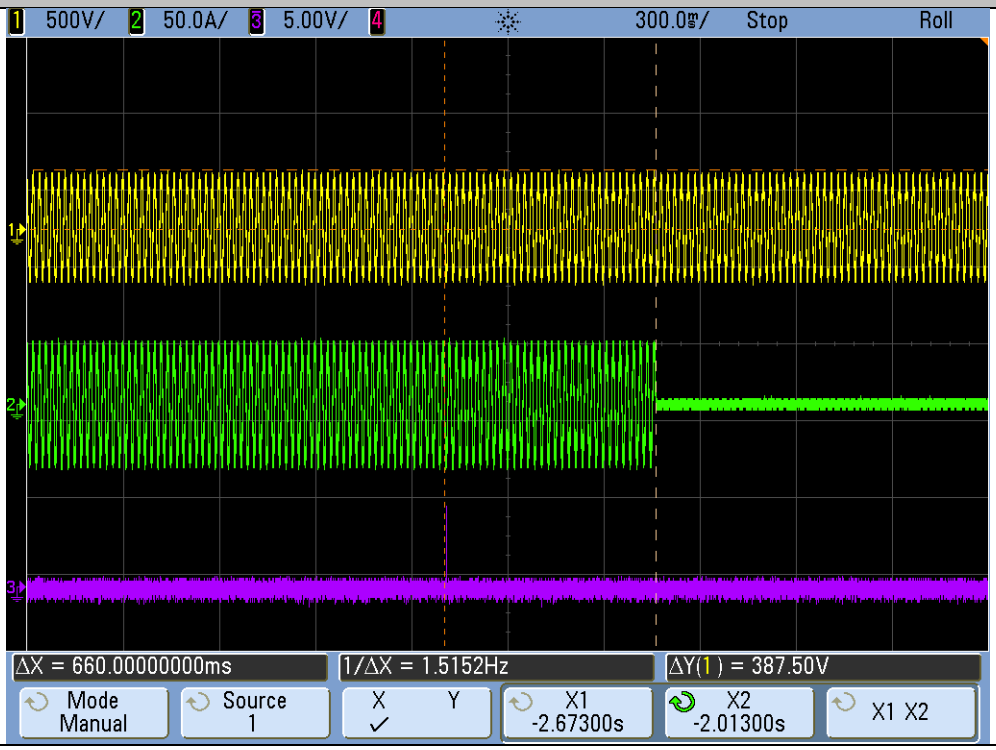
Under frequency, Stage 2 - Test 2



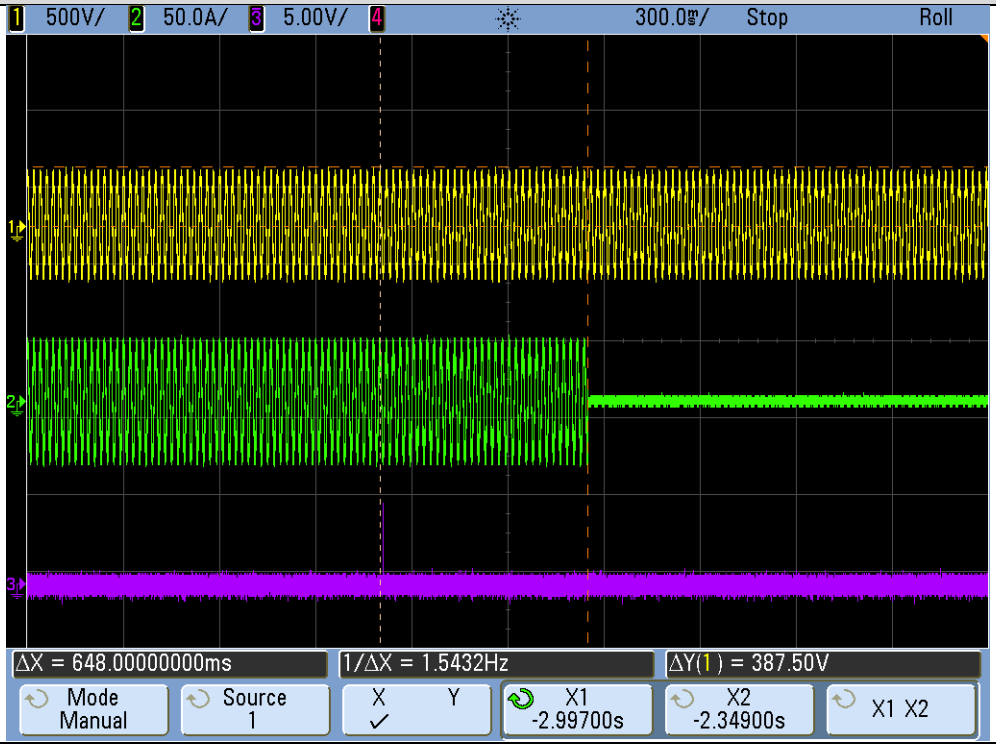
Under frequency, Stage 2 - Test 3



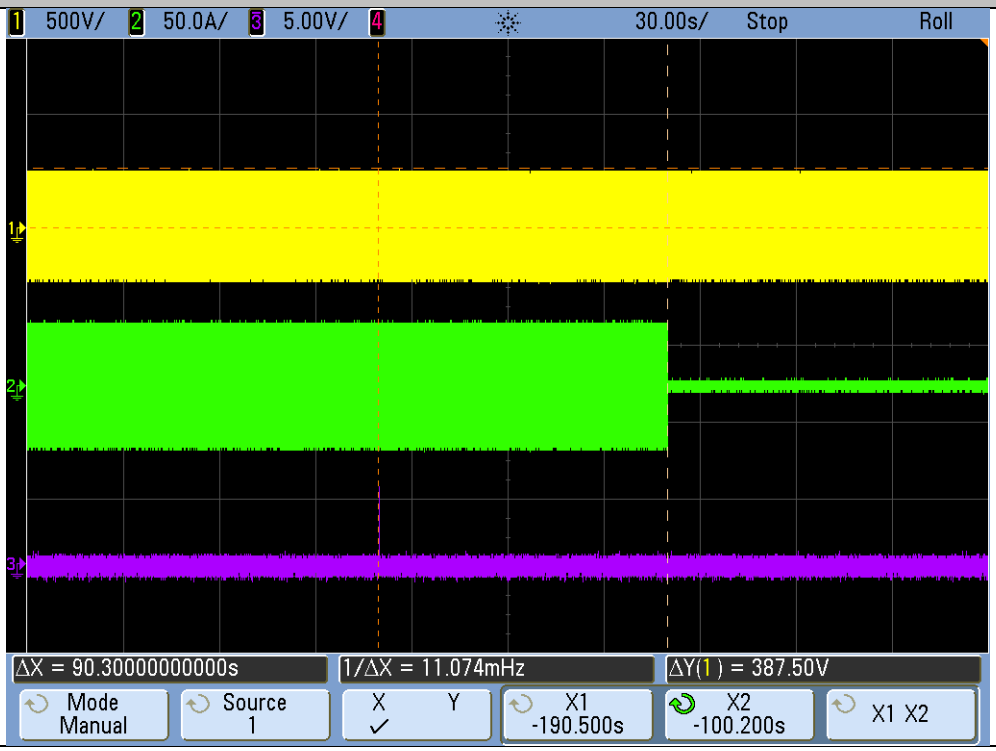
Under frequency, Stage 2 - Test 4



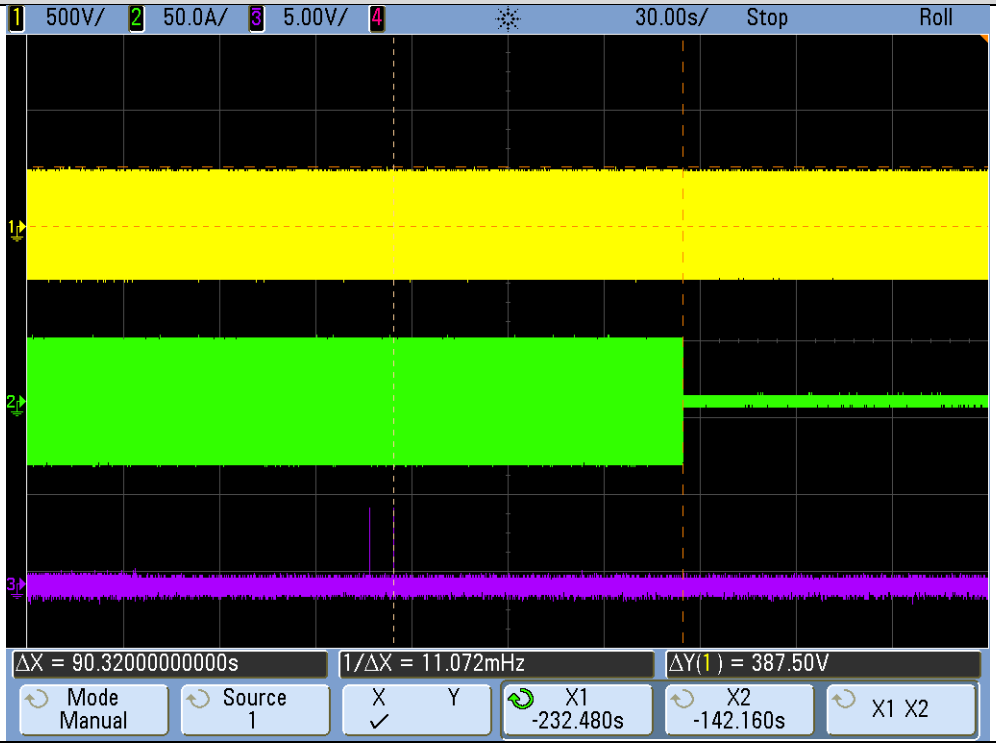
Under frequency, Stage 2 - Test 5



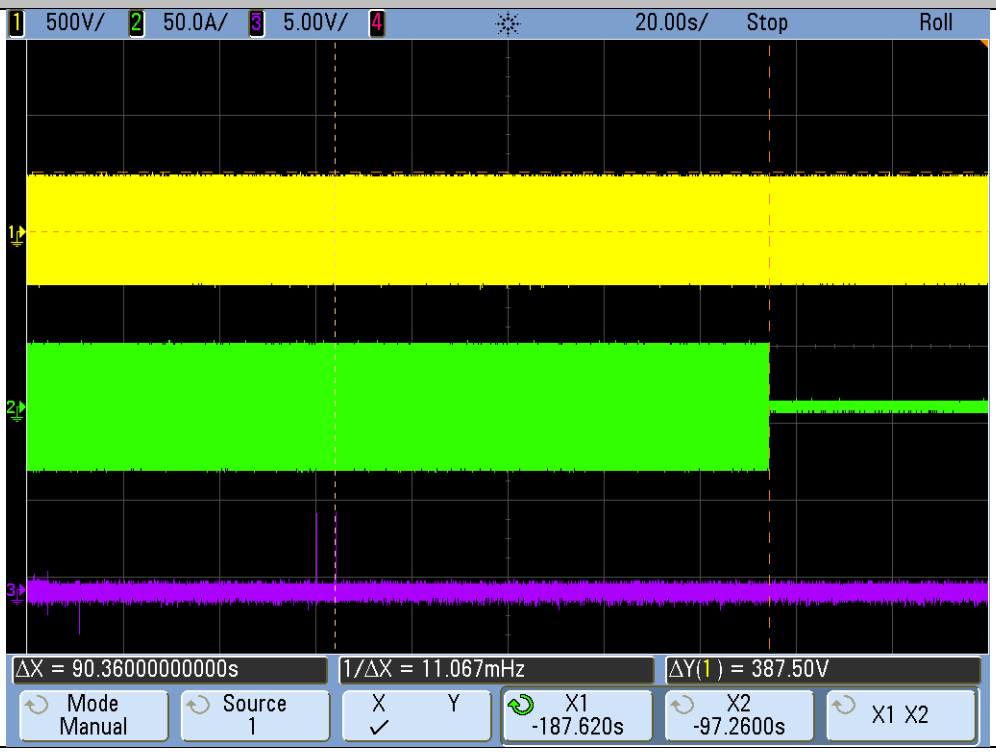
Over frequency, Stage 1 - Test 1



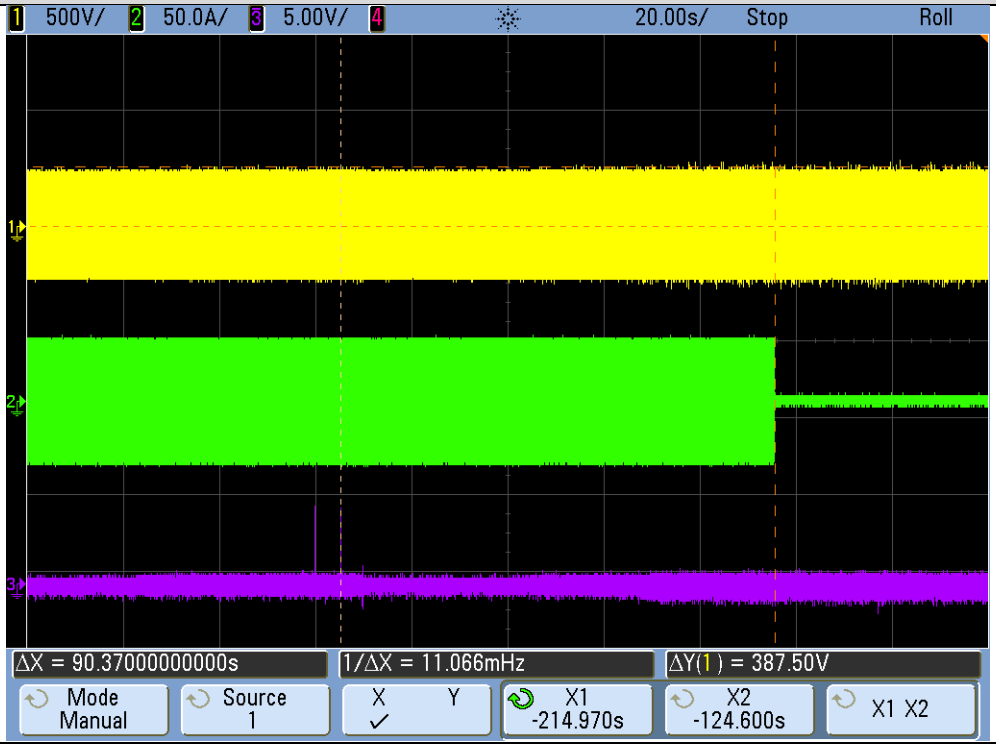
Over frequency, Stage 1 - Test 2



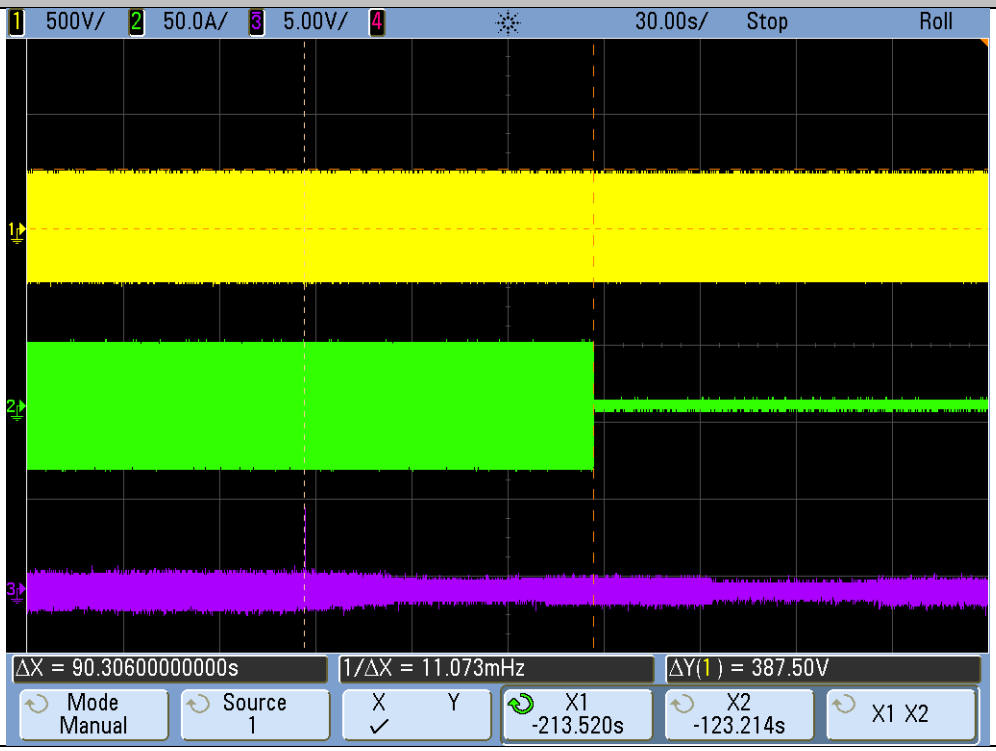
Over frequency, Stage 1 - Test 3



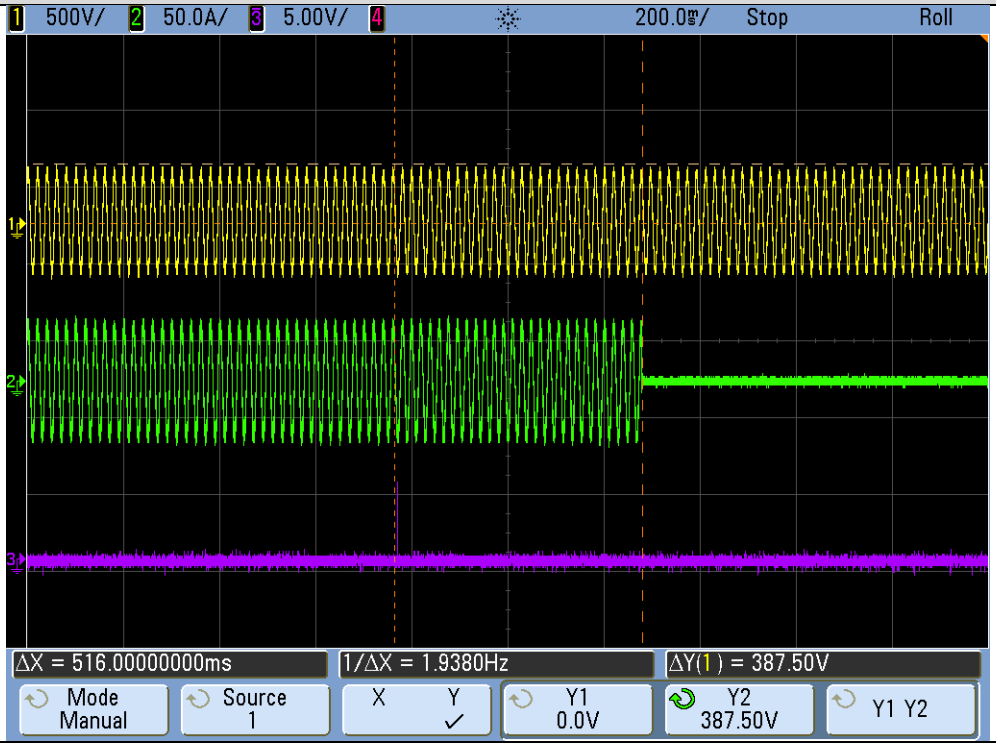
Over frequency, Stage 1 - Test 4



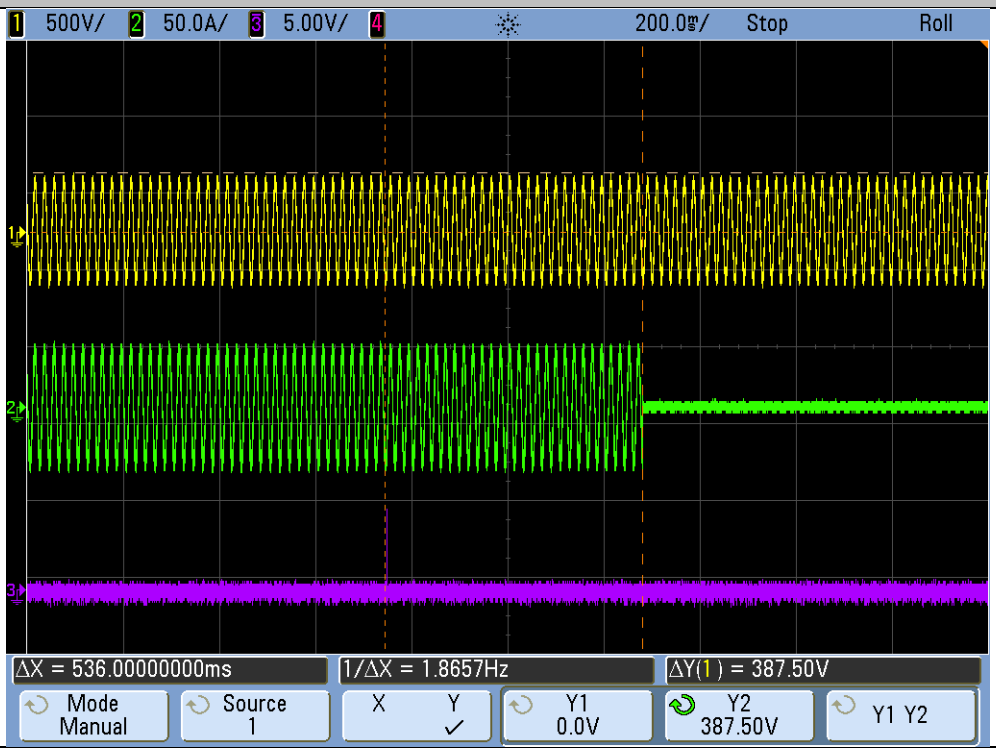
Over frequency, Stage 1 - Test 5



Over frequency, Stage 2 - Test 1

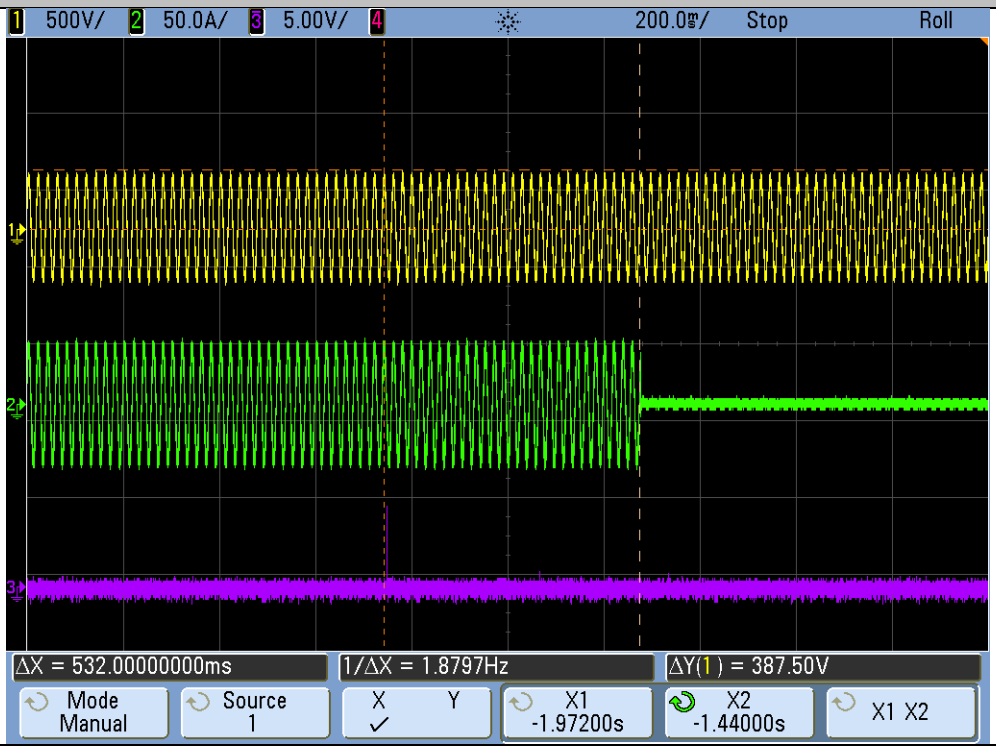


Over frequency, Stage 2 - Test 2

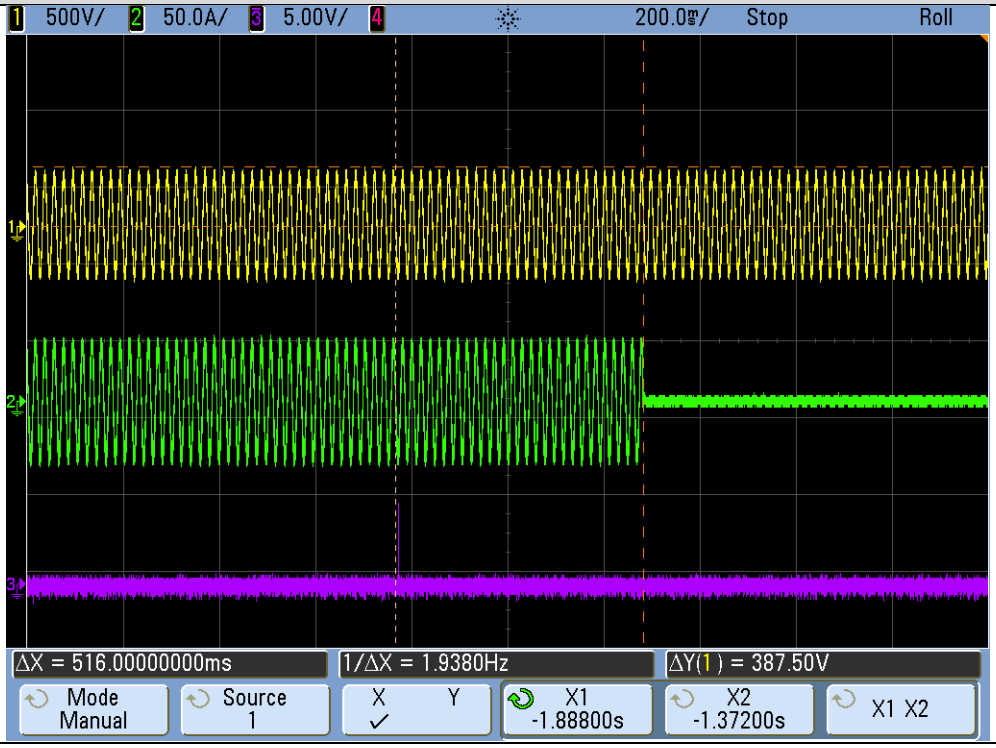


Over frequency, Stage 2 - Test 3

Over frequency, Stage 2 - Test 4



Over frequency, Stage 2 - Test 5



4.1.4 No trip Tests

No trip tests have been done according to the point 13.8.3.2 and tables of the chapter 13.1 of the standard.

To ensure that the protection will not trip in error voltage and frequency, “no-trip tests” have been carried out at frequencies, voltages and time configurations detailed bellow.

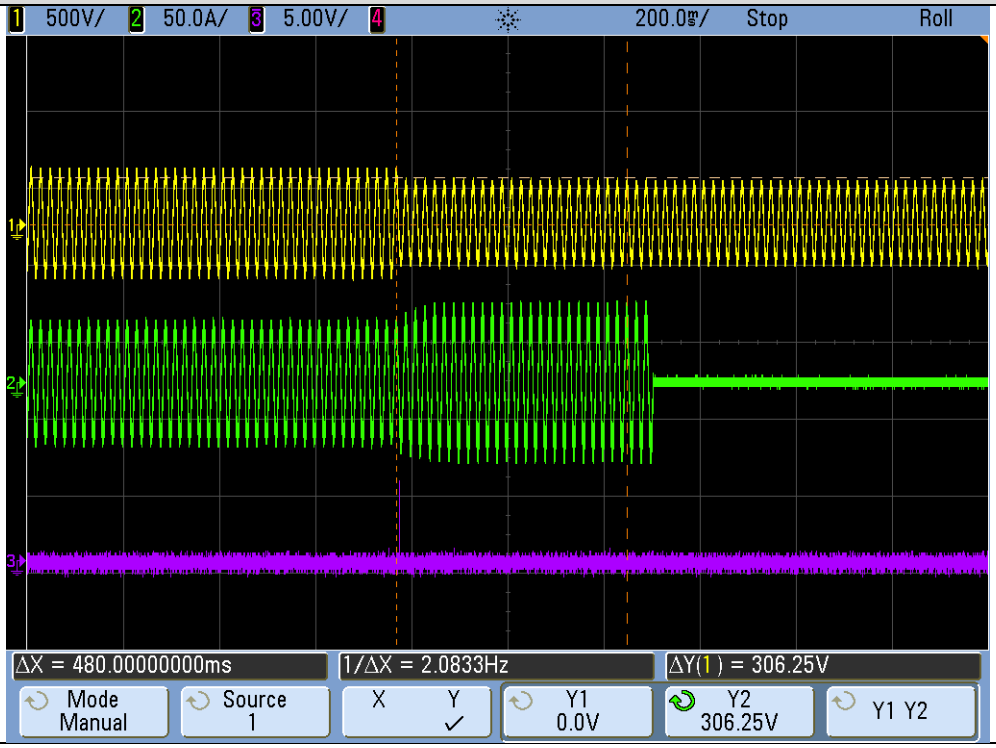
The test procedure consists in leading the inverter out from its normal conditions with a step to the set-point of frequency or voltage established at the tables below and maintain the step for the time desired, once reached the time desired the inverter is taken back to the normal conditions, the inverter shall not trip during the test.

4.1.4.1 Voltage no-trip tests

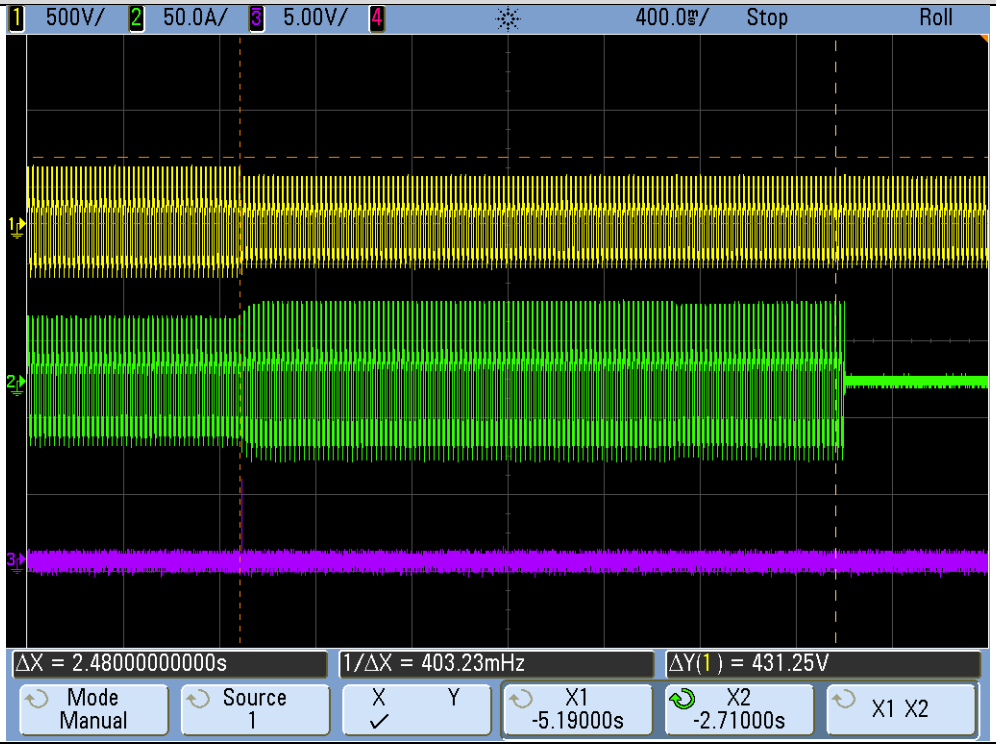
Test No	Voltage setting (V)	Time required (s)	Time measured (s)	Disconnection
1	180.0	0.48	0.48	☒ NO ☐ YES
2	188.0	2.48	2.48	☒ NO ☐ YES
3	204.1	3.5	3.5	☒ NO ☐ YES
4	258.2	2.0	2.0	☒ NO ☐ YES
5	269.7	0.98	0.98	☒ NO ☐ YES
6	277.7	0.48	0.48	☒ NO ☐ YES

Test results are graphically shown in following pages.

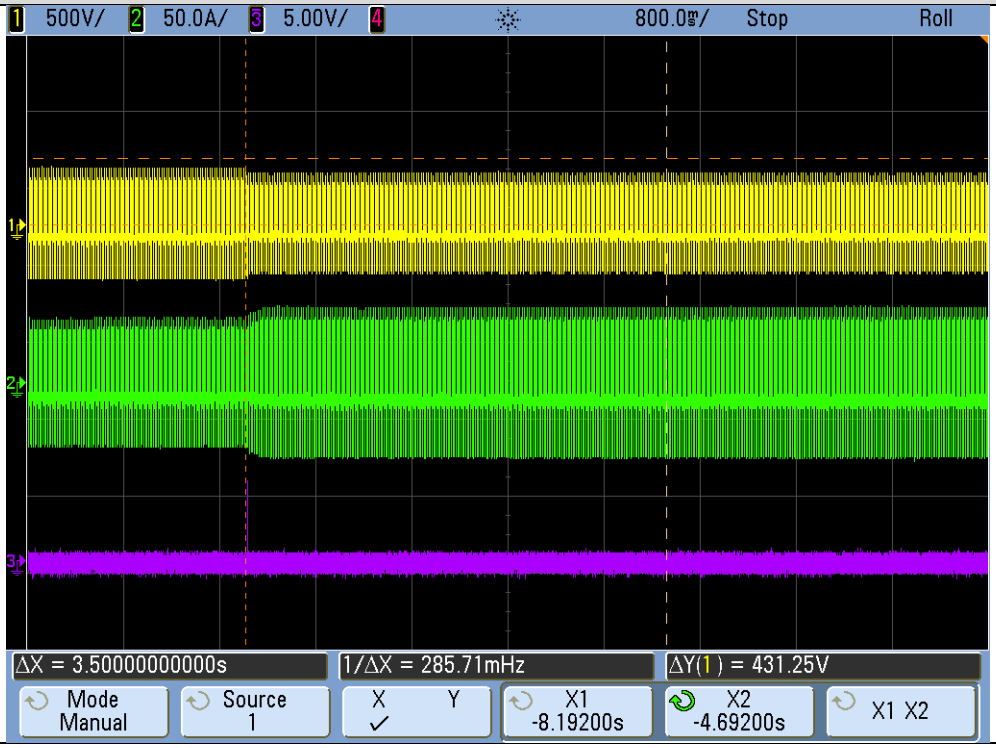
Voltage no-trip tests - Test 1



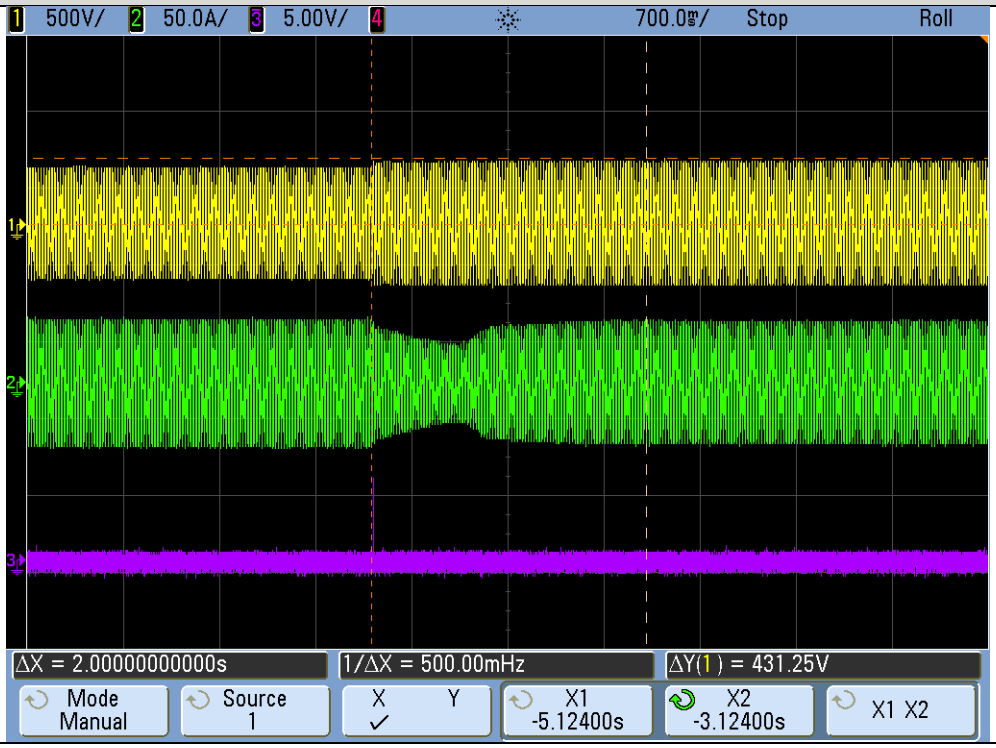
Voltage no-trip tests - Test 2



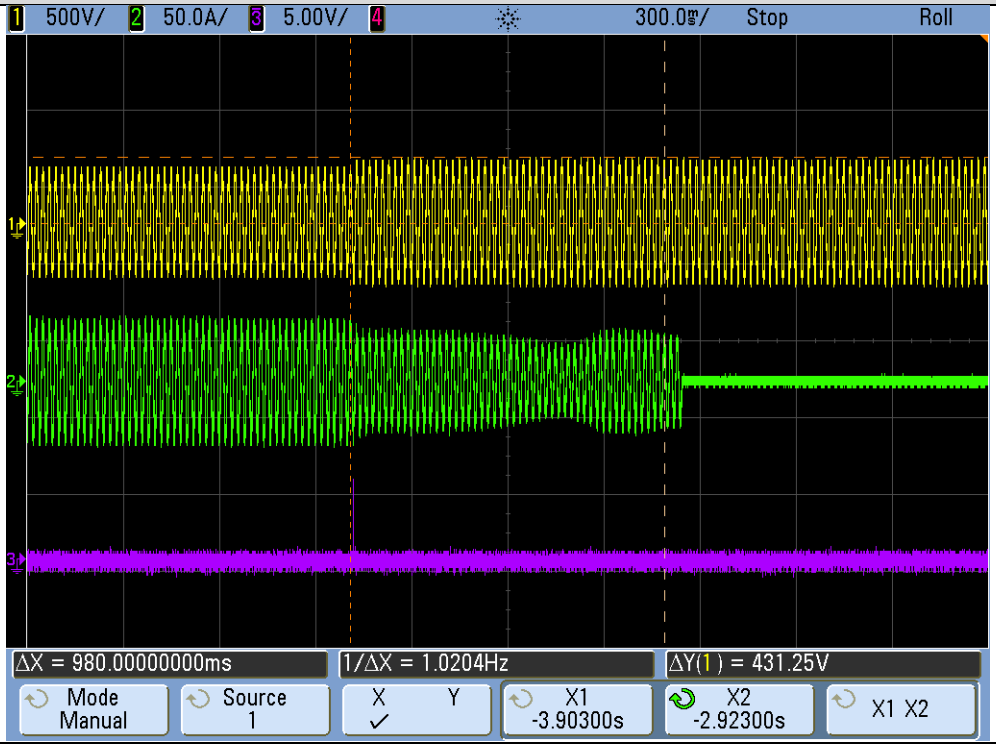
Voltage no-trip tests - Test 3



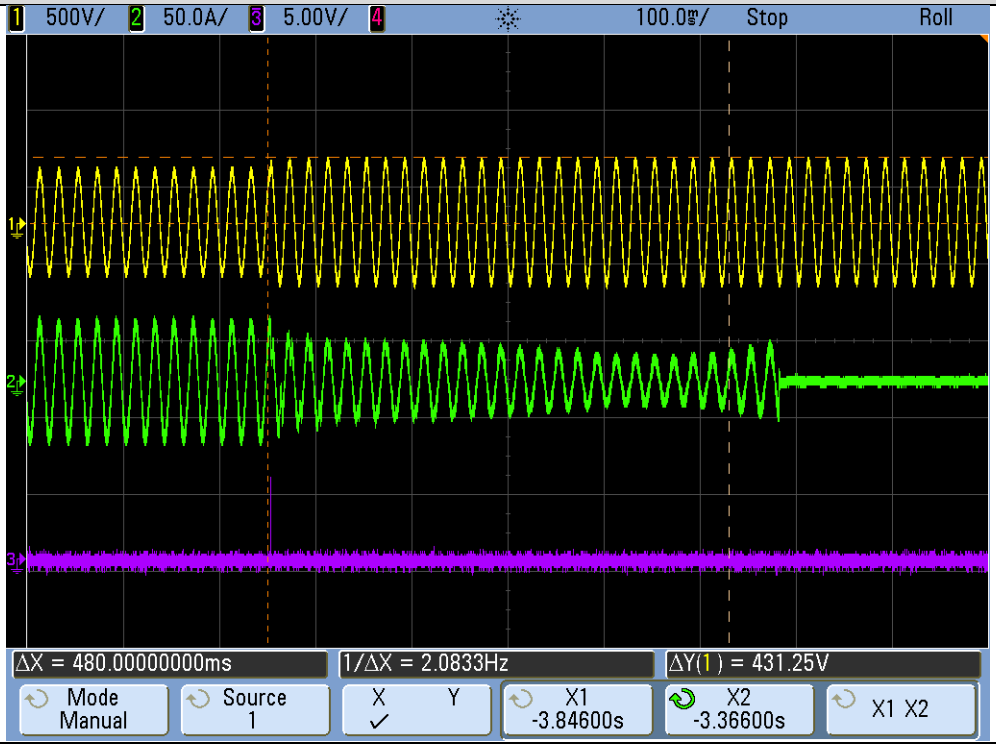
Voltage no-trip tests - Test 4



Voltage no-trip tests - Test 5



Voltage no-trip tests - Test 6

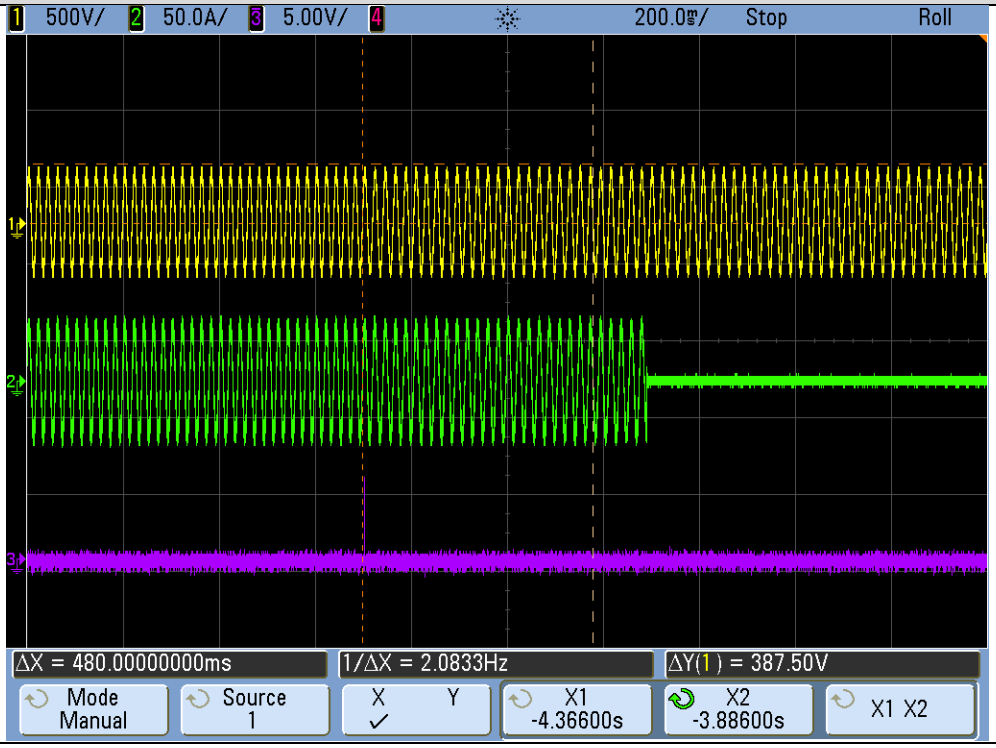


4.1.4.2 Frequency no-trip tests

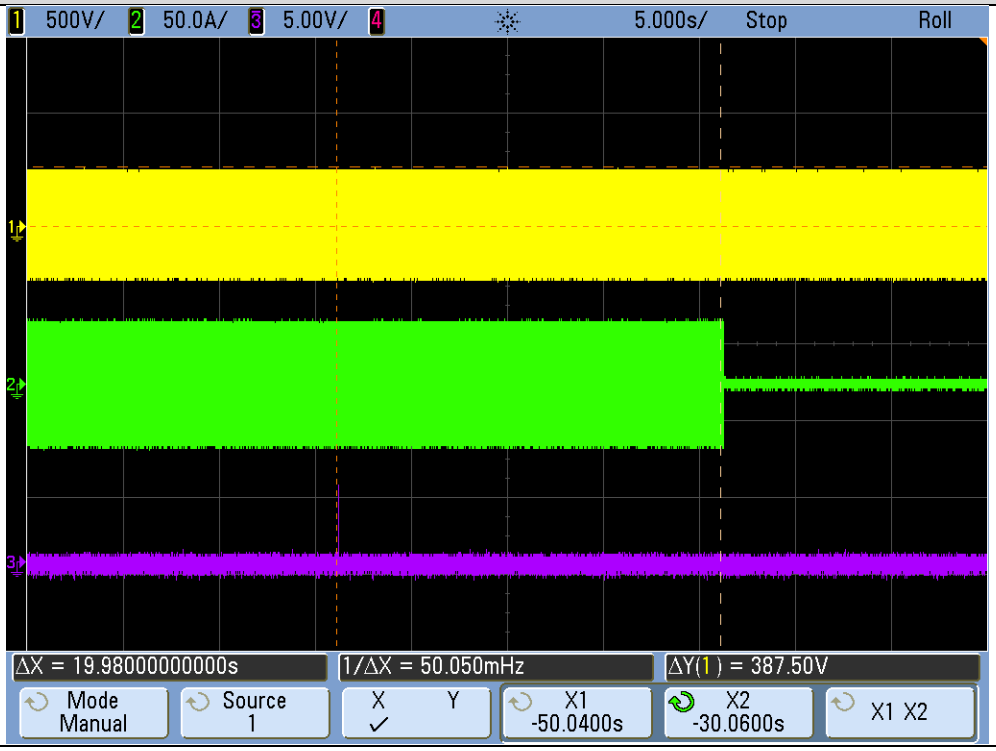
Test No.	Frequency setting (Hz)	Time required (s)	Time measured (s)	Disconnection
1	46.8	0.48	0.48	☒ NO ☐ YES
2	47.2	19.98	19.98	☒ NO ☐ YES
3	47.7	25	25	☒ NO ☐ YES
4	51.3	95	95	☒ NO ☐ YES
5	51.8	89.98	89.98	☒ NO ☐ YES
6	52.2	0.48	0.48	☒ NO ☐ YES

Test results are graphically shown in following pages.

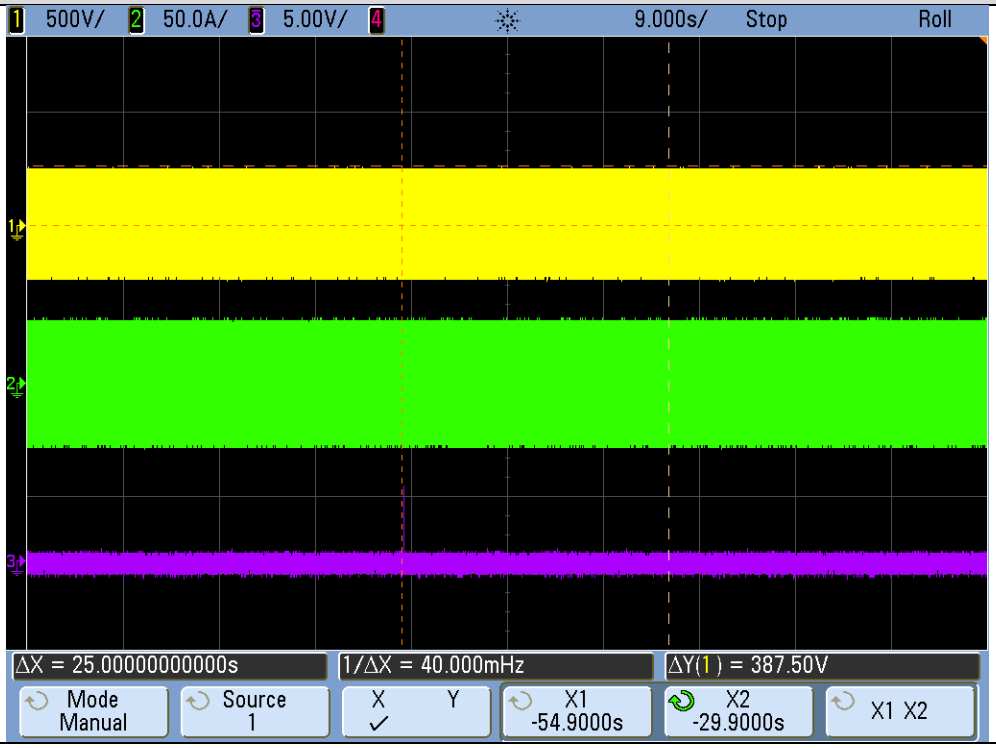
Frequency no-trip tests - Test 1



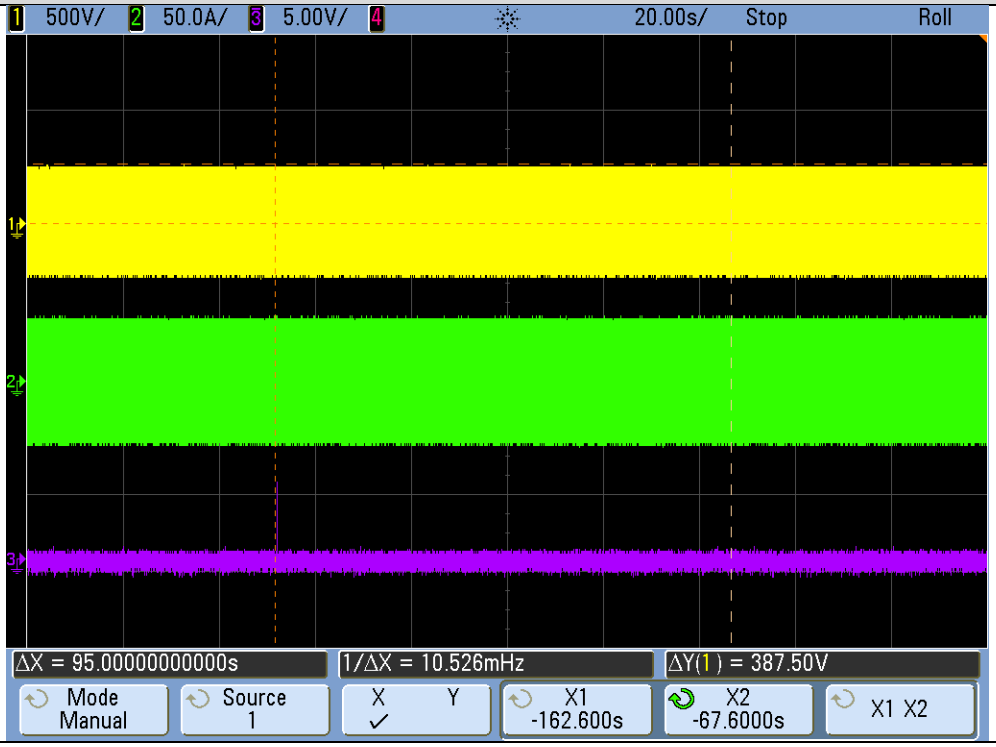
Frequency no-trip tests - Test 2



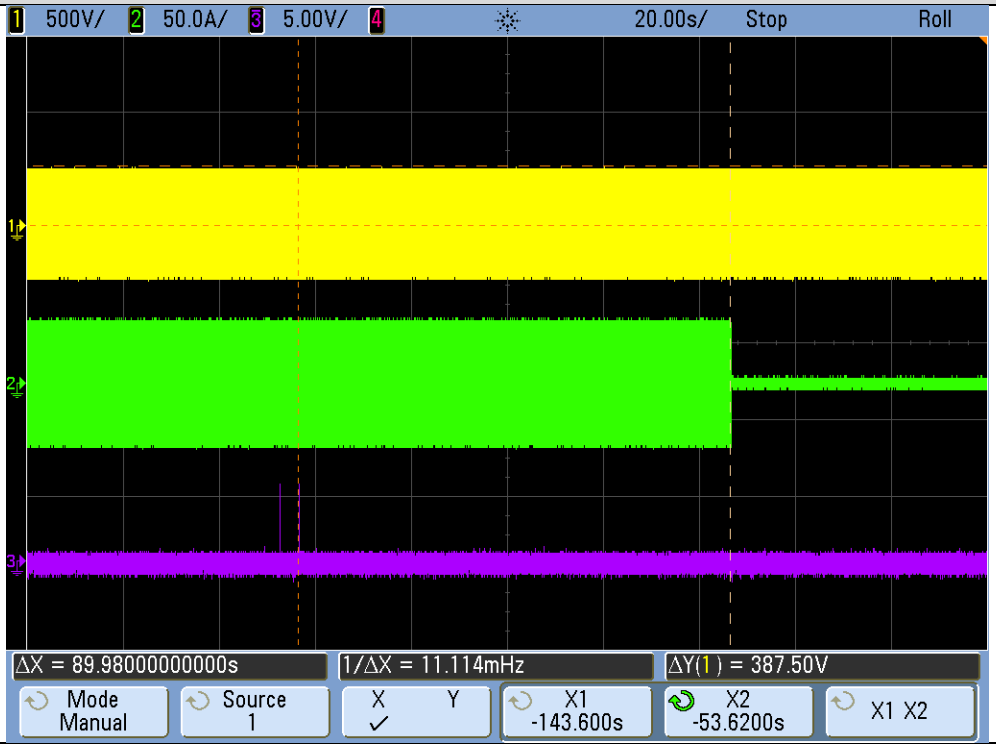
Frequency no-trip tests - Test 3



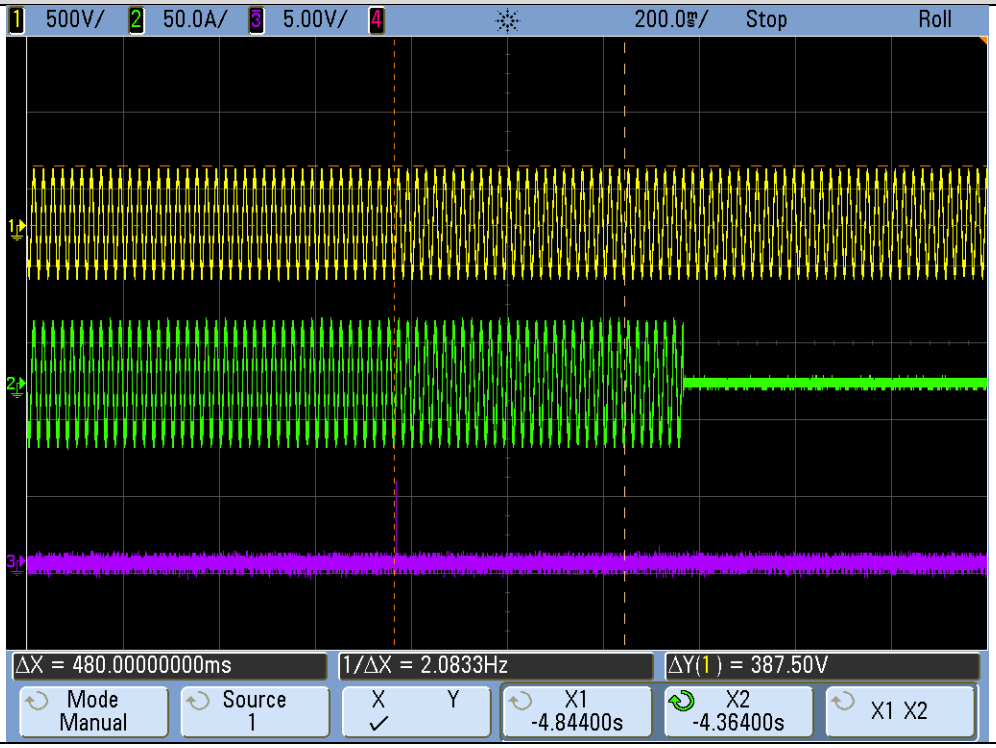
Frequency no-trip tests - Test 4



Frequency no-trip tests - Test 5



Frequency no-trip tests - Test 6



4.1.5 Loss of Mains test

The test has been done according to point 13.8.3.4A of the standard.

Loss of Mains test has been carried out with the set up specified in the point 2.6 of this report, using the grid and RLC load bank at the AC side.
With a switch located between EUT/RLC bank and the grid is possible to do a loss of mains condition. Test has been done according to IEC 62116.

The compliances with these requirements are stated in the following test report:

- IEC 62116: test report nº 2217 / 1094-1

Note: Trip time limit is 1.0 seconds.

4.1.6 Reconnection

Test performed according to the point 13.8.3.5 of the standard.

The inverter shall only automatically reconnect when the voltage and frequency levels are within the stage 1 protection function limits. The minimum reconnection delay shall be at least 20 seconds

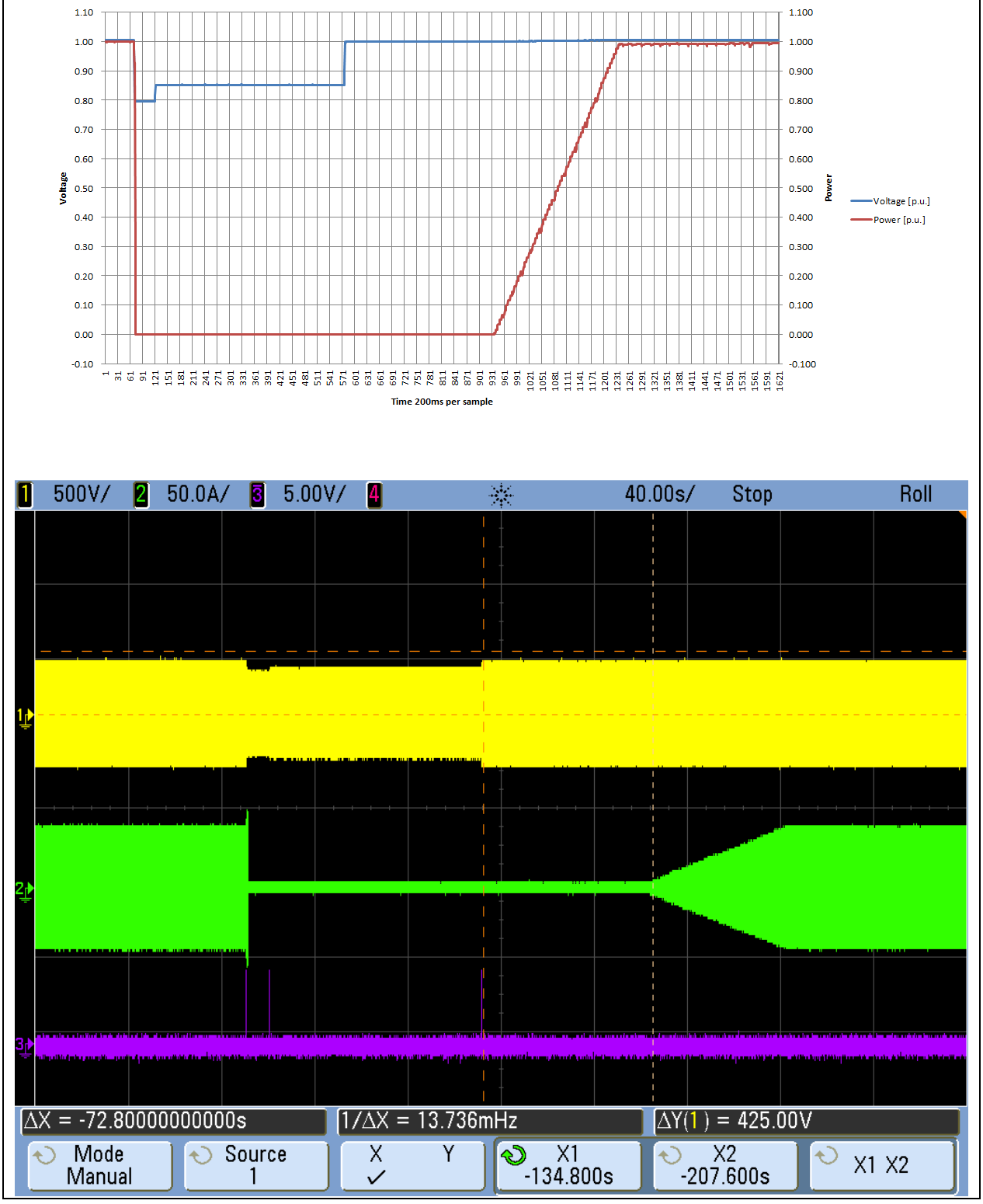
4.1.6.1 Voltage Reconnection Conditions

The three phases are adjusted to the same voltage level for this test. The following table detail tests performed.

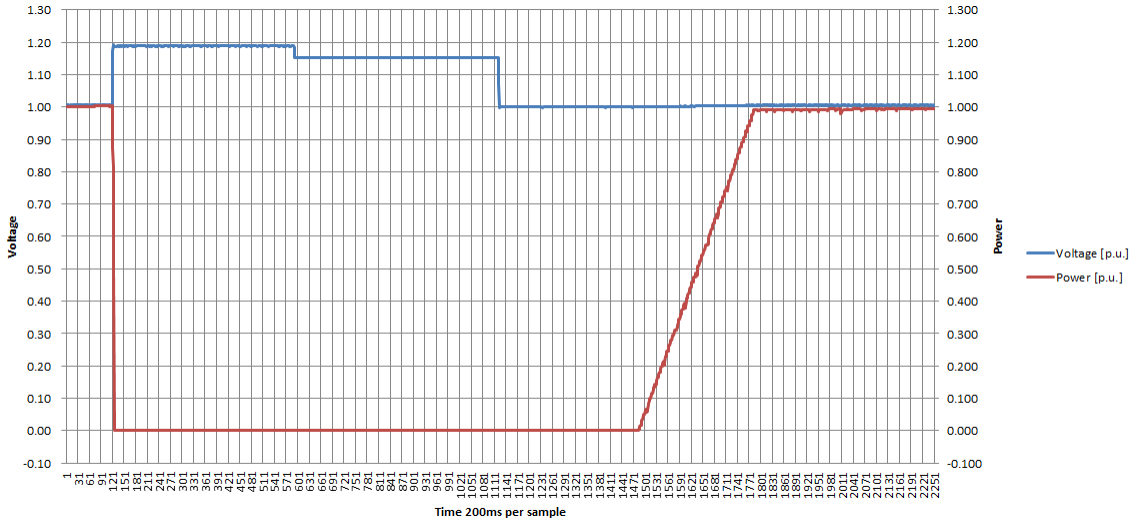
Test at	Time delay setting(s)	Measured delay(s)	Checks on no reconnection when voltage is brought to just outside stage 1 limits of table 1.	
UV	65	72.8	At 266.2V	At 196.1V
OV	65	71.2		
Confirmation that the SSEG does not re-connect.			Not reconnection	Not reconnection

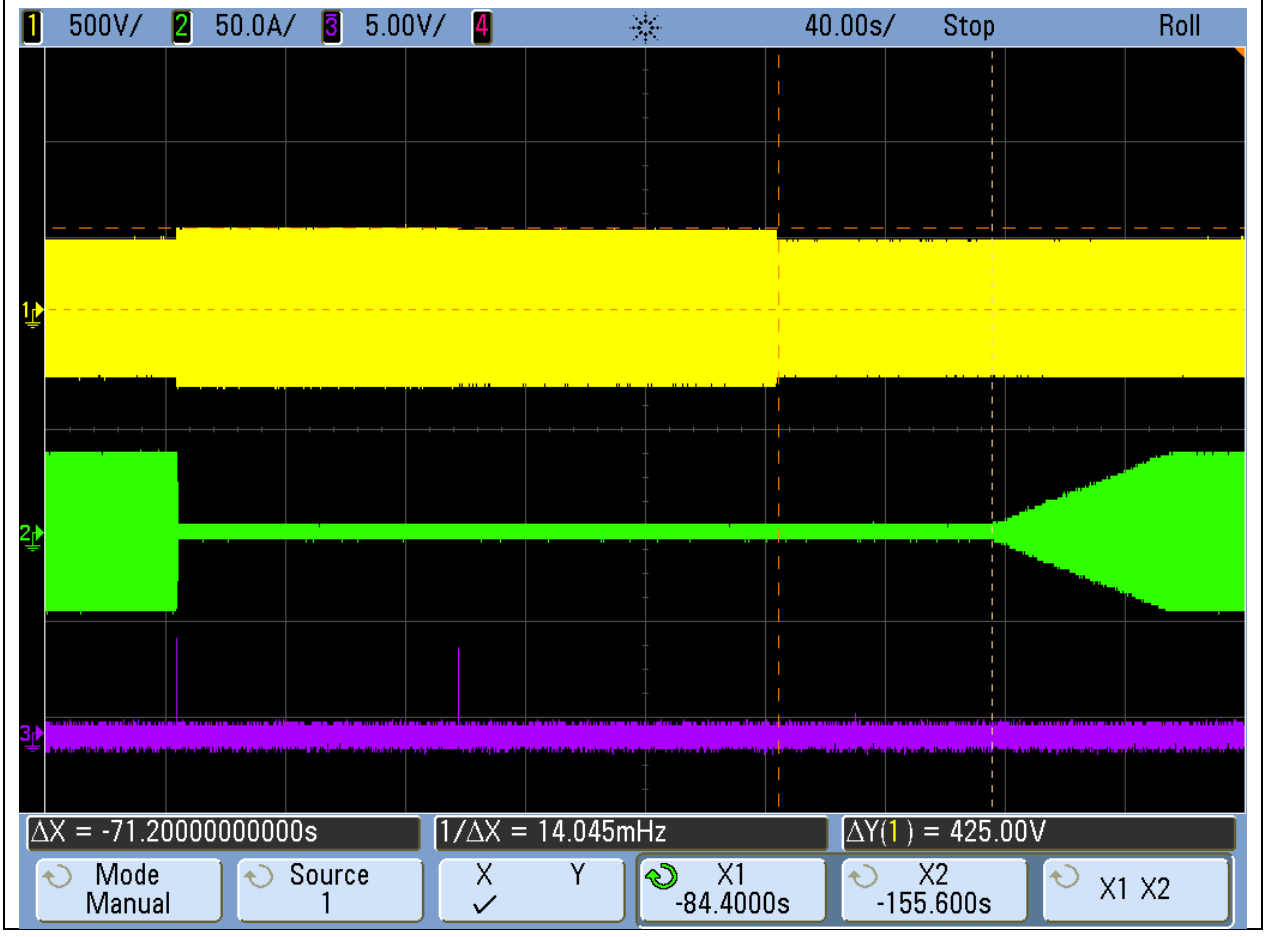
Test results are graphically shown below.

Under voltage reconnection



Over voltage reconnection





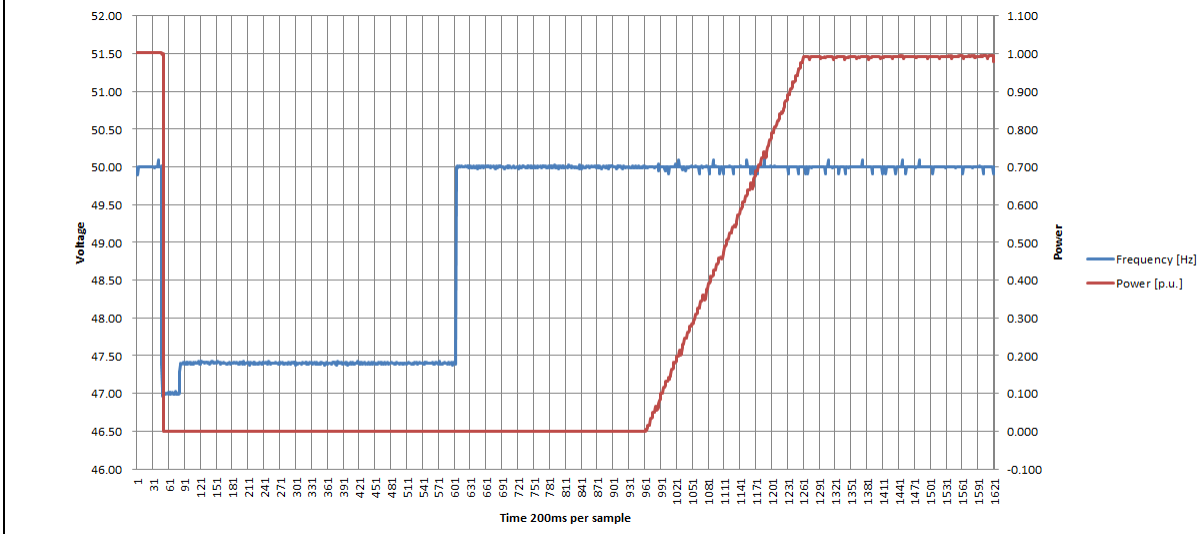
4.1.6.2 Frequency Reconnection Conditions

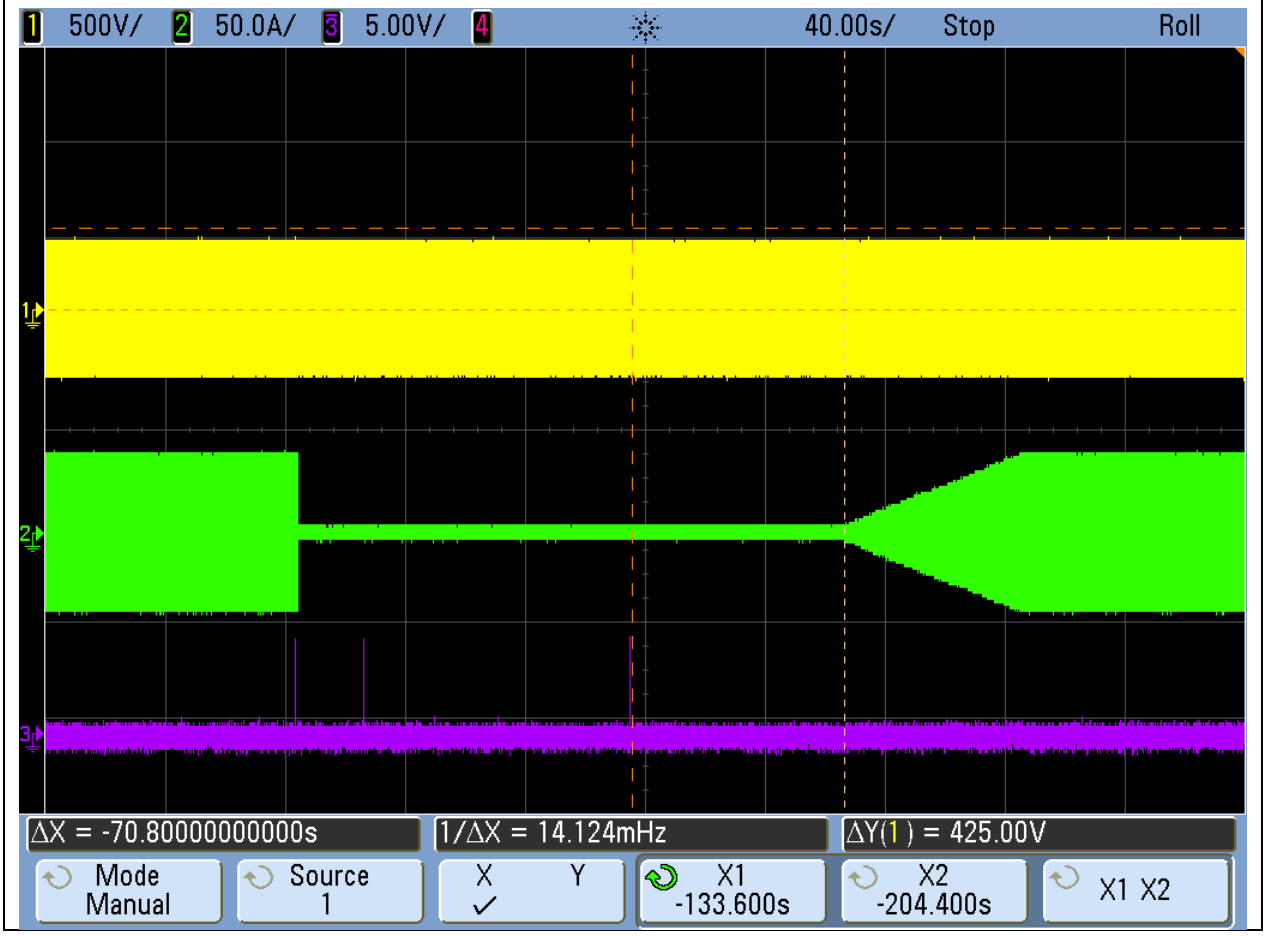
The following table detail tests performed.

Test at	Time delay setting	Measured delay(*)	Checks on no reconnection when frequency is brought to just outside stage 1 limits of table 1.	
UF	65s	70.8	At 47.4Hz	At 51.6Hz
OF	65s	70.0		
Confirmation that the SSEG does not re-connect.			Not reconnection	Not reconnection

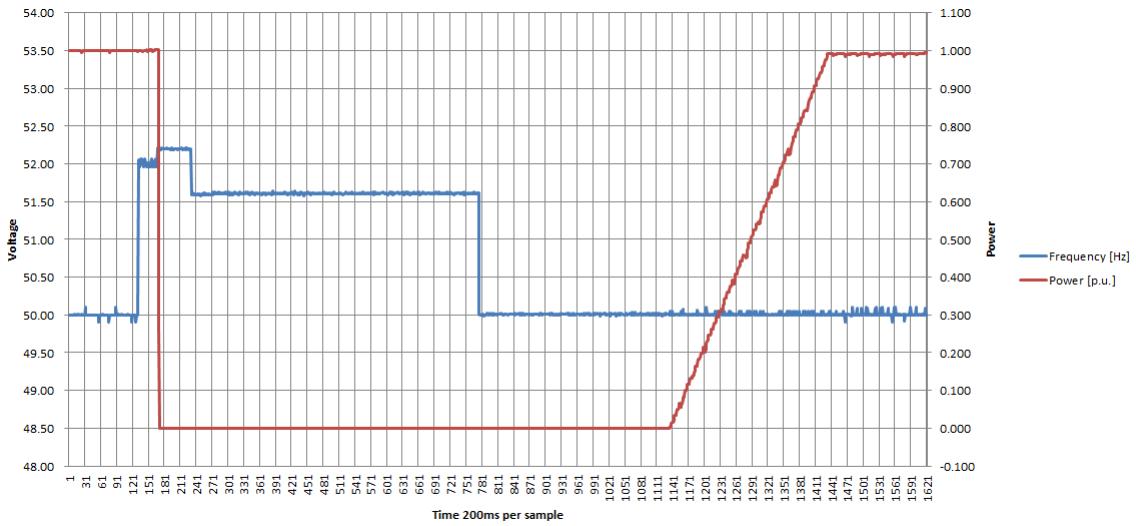
Test results are graphically shown below.

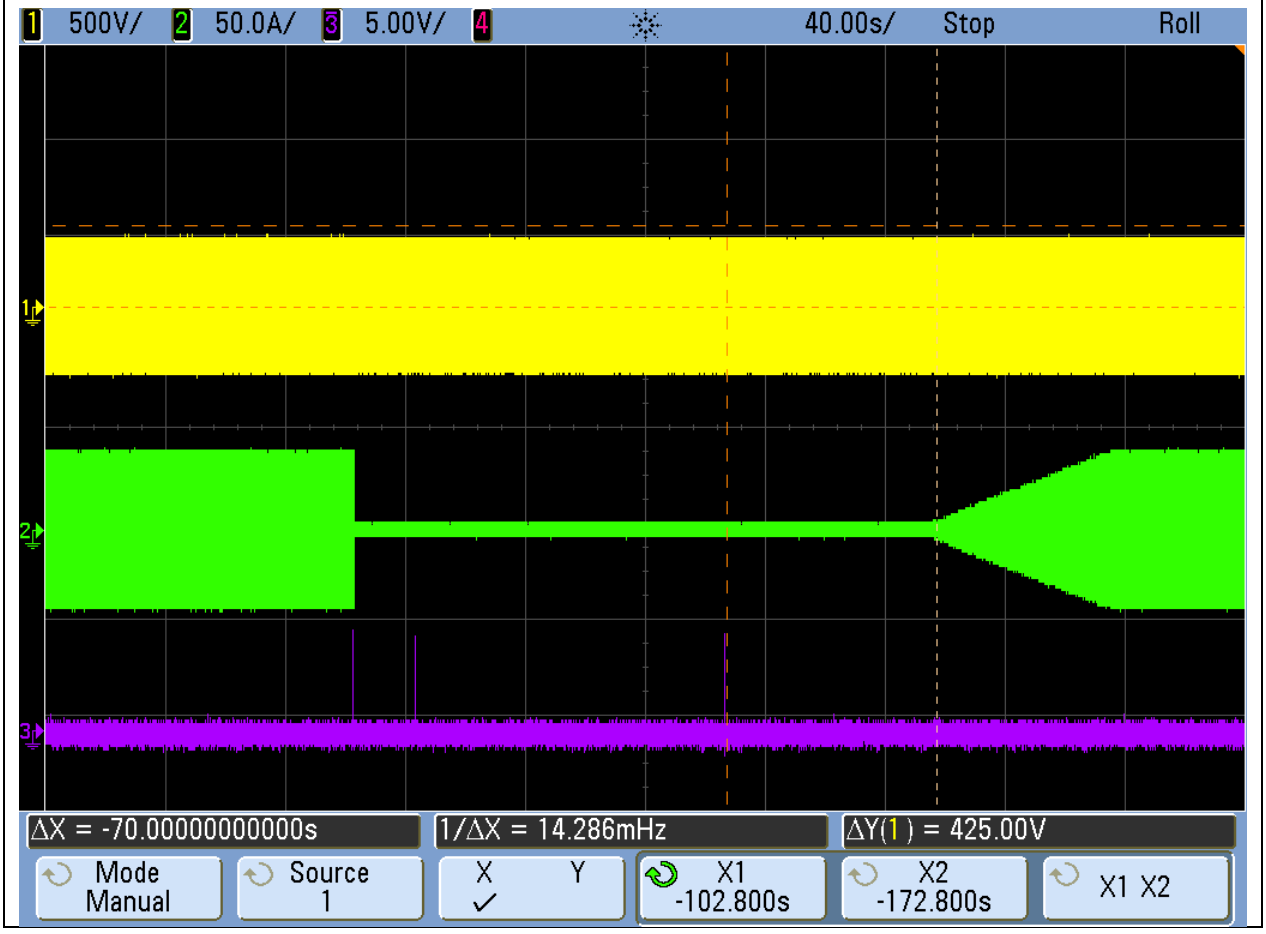
Under frequency reconnection





Over frequency reconnection





4.1.7 Frequency drifts and step changes.

These tests have been performed according to the point 13.8.3.6 of the standard, using the AC Source as variable frequency supply to the inverter. The AC source generates negative and positive ramps/steps of frequency and the inverter shall not disconnect.

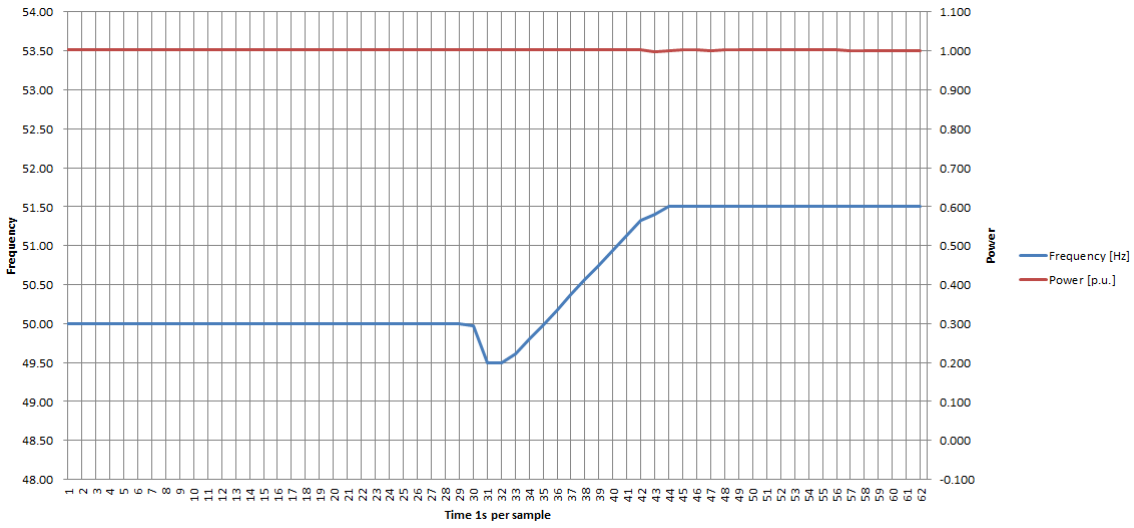
4.1.7.1 Frequency drift test

The following table detail tests performed.

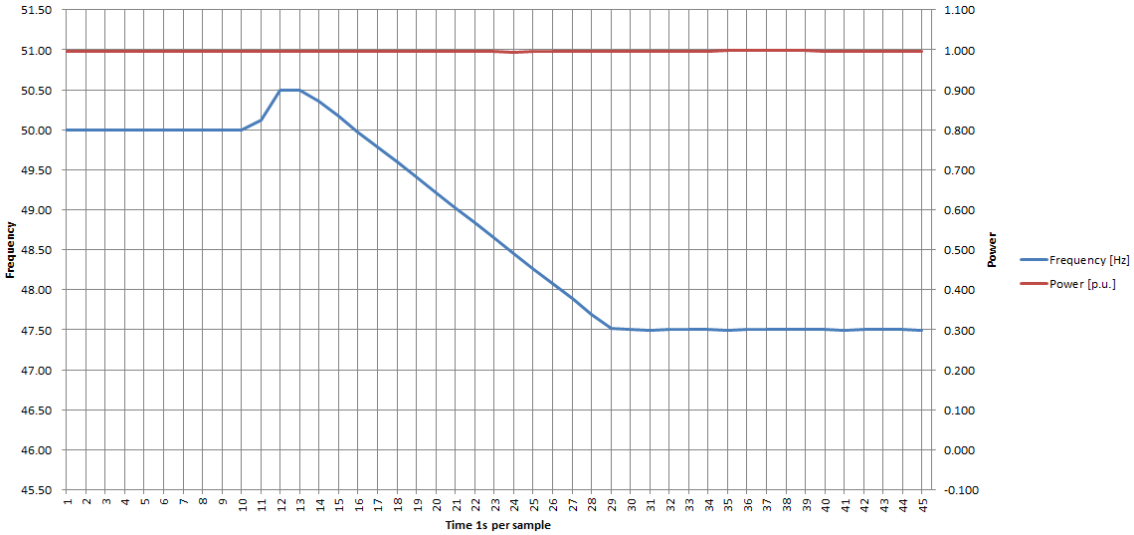
	Start frequency (Hz)	Change desired (Hz/s)	Final Value (Hz)	Time Change (s)	Ramp measured (Hz/s)	Disconnection
Positive frequency drift	49.5	+0.19	51.4	10	+0.19	☒ NO ☐ YES
Negative frequency drift	50.5	-0.19	47.5	16	-0.19	☒ NO ☐ YES

Test results are graphically shown in following pages.

Positive frequency drift



Negative frequency drift



4.1.7.2 Vector shift test.

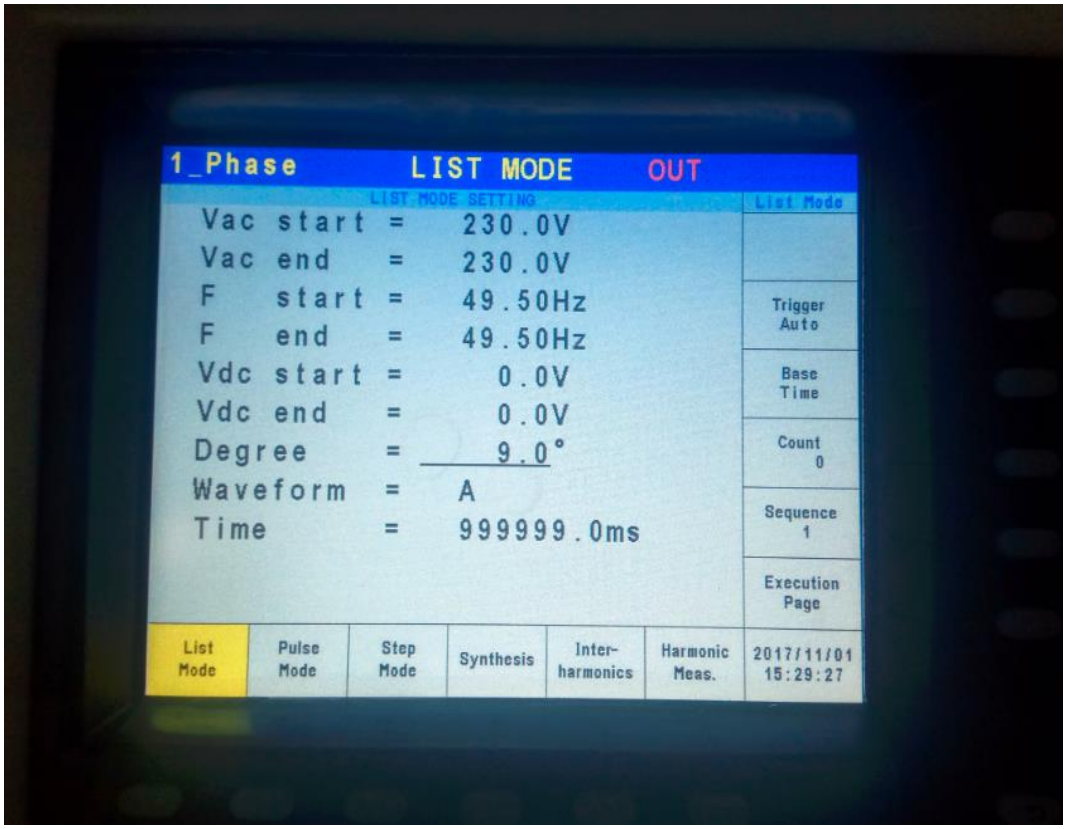
This test has been performed programming with 9º vector shift in a voltage cycle and the inverter shall not disconnect.

	Start frequency	Jump Performed	Final Frequency (Hz)	Disconnection
Positive Vector Shift	49.5Hz	+9 degrees		☒ NO ☐ YES
Negative Vector Shift	50.5Hz	-9 degrees		☒ NO ☐ YES

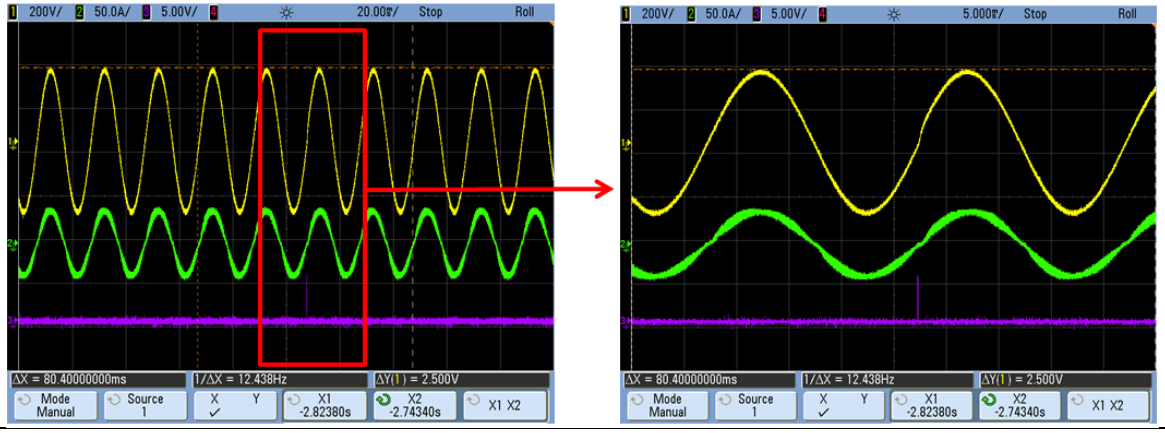
Test results are graphically shown below.

Positive Vector Shift

Setting:

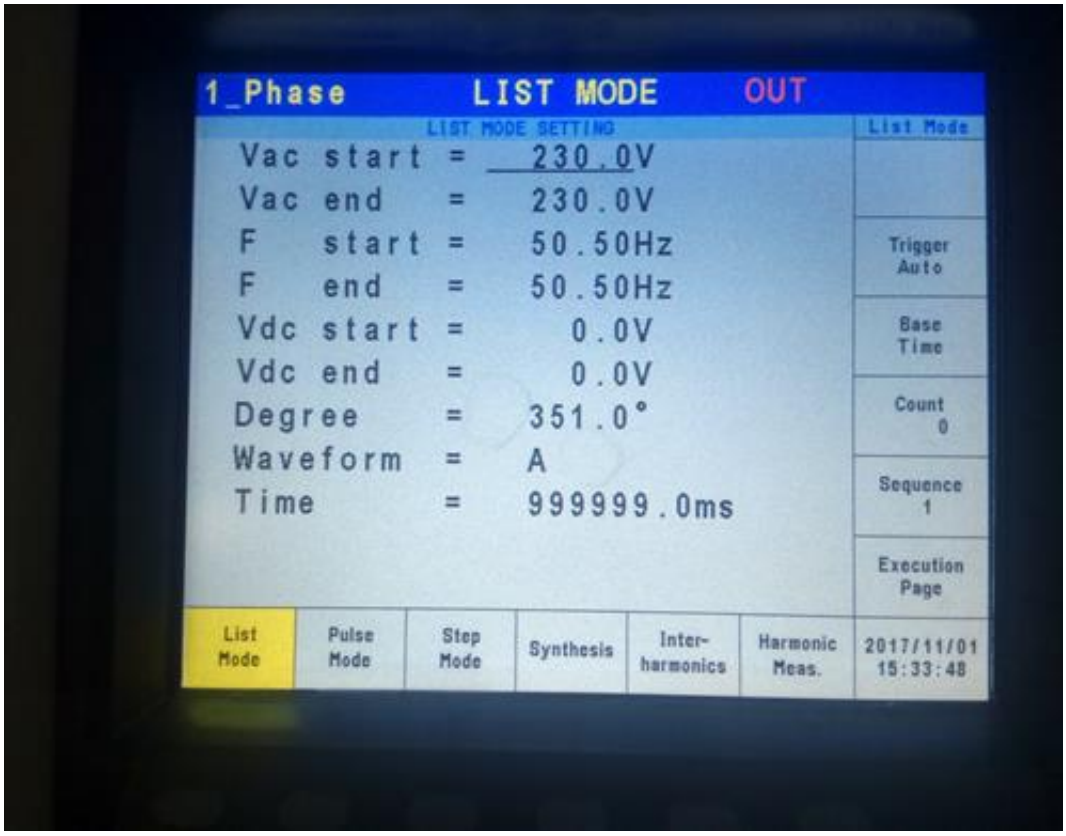


Measured result:

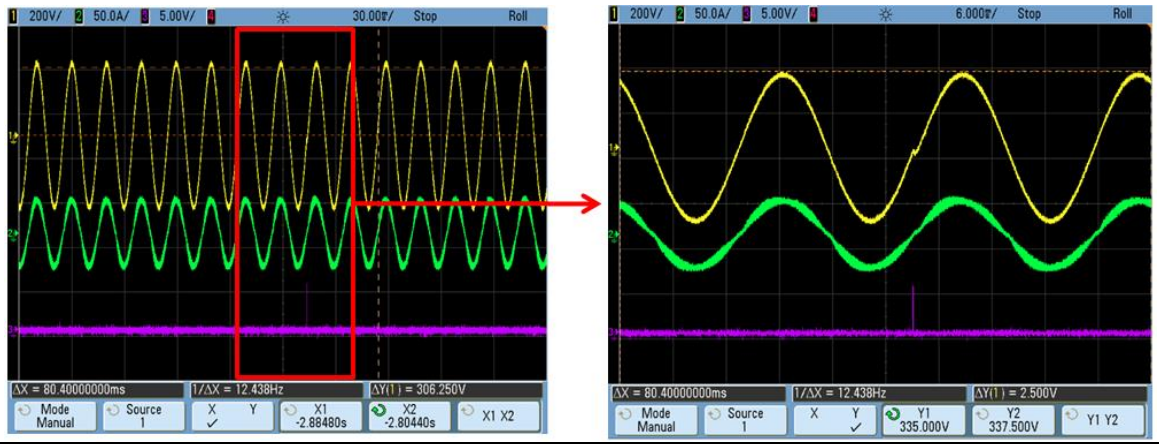


Negative Vector Shift

Setting:



Measured result:



4.2 POWER QUALITY

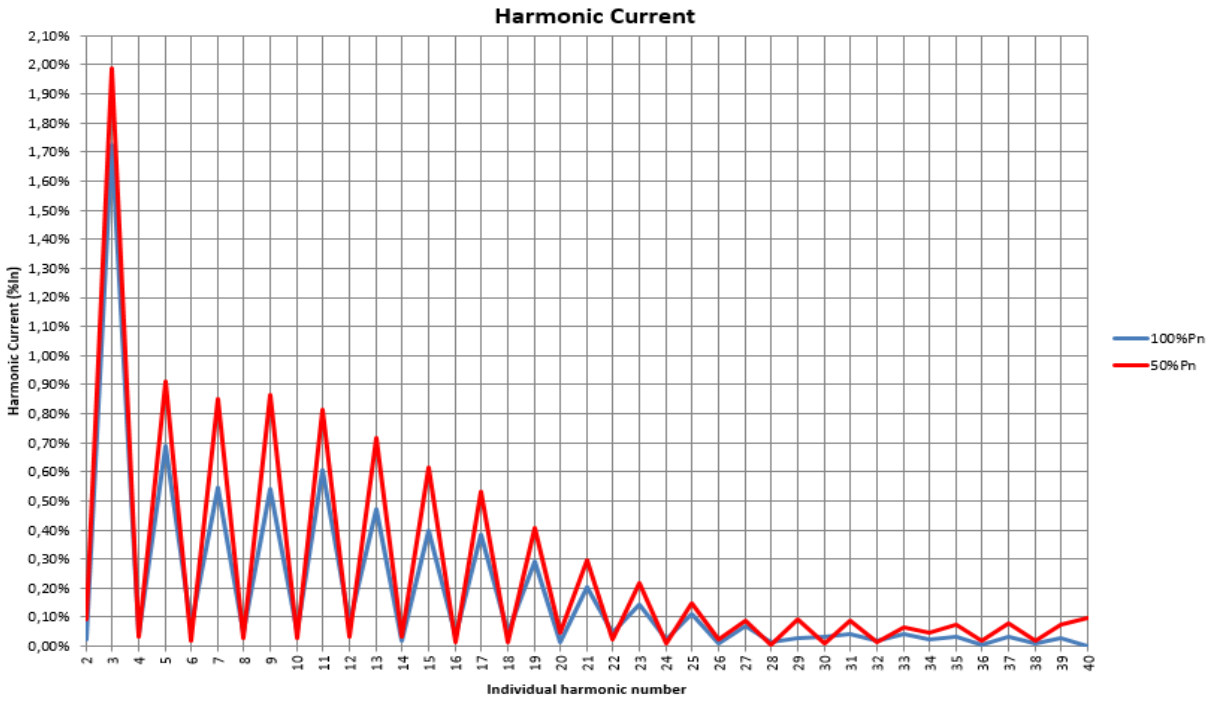
4.2.1 Current Harmonics

Harmonics measures have been performed according to the point 13.8.4.1 and regarding the procedures specified by BS EN 61000-3-12.

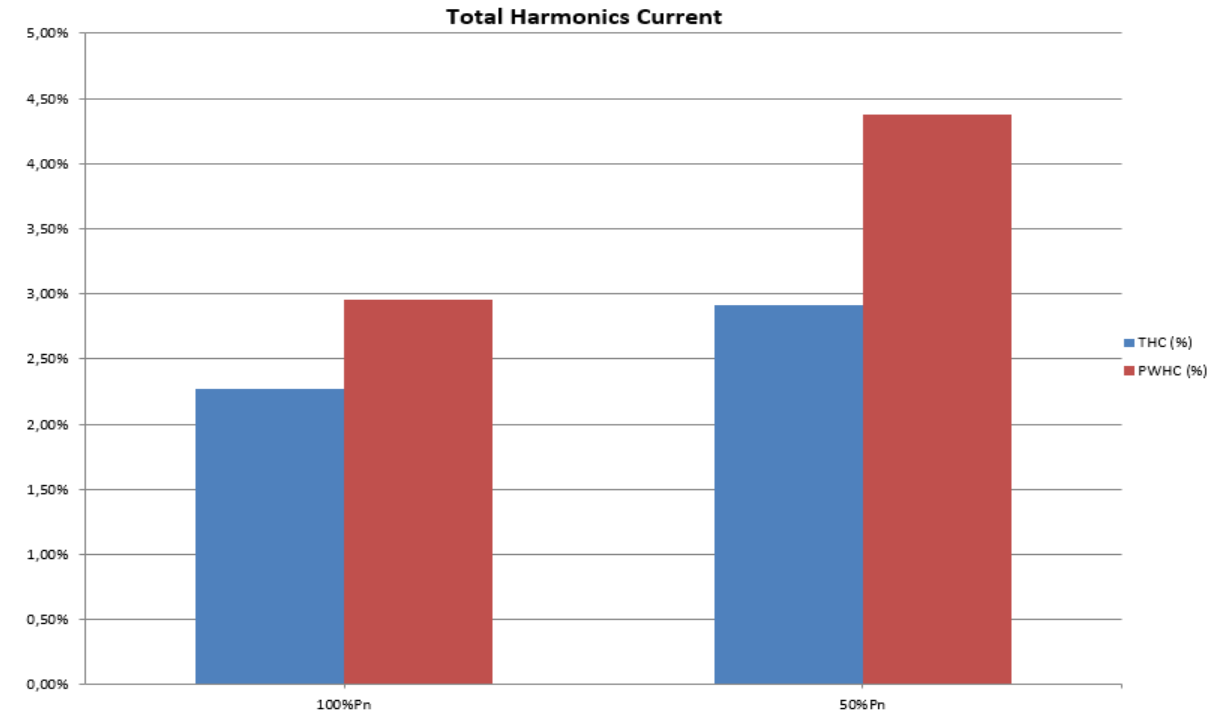
Measures have been repeated at 50%P_n and 100%P_n.

CS2000			Harmonic % =Measured Value (Amps) x 23/rating per phase (kVA)		
P_n (%)	50		100		LIMIT (%)
Nr./Order	I_h(A)	I_h(%)	I_h(A)	I_h(%)	
2	0.012	0.095	0.006	0.024	8.0
3	0.260	1.990	0.449	1.725	--
4	0.004	0.031	0.011	0.041	4.0
5	0.119	0.910	0.180	0.691	10.7
6	0.003	0.021	0.018	0.071	2.7
7	0.111	0.851	0.142	0.547	7.2
8	0.003	0.026	0.012	0.045	2.0
9	0.113	0.863	0.141	0.540	--
10	0.004	0.029	0.014	0.053	1.6
11	0.106	0.812	0.158	0.607	3.1
12	0.004	0.031	0.020	0.078	1.3
13	0.094	0.719	0.123	0.473	2.0
14	0.005	0.035	0.005	0.020	--
15	0.080	0.616	0.104	0.398	--
16	0.002	0.013	0.010	0.038	--
17	0.069	0.530	0.100	0.383	--
18	0.002	0.015	0.012	0.048	--
19	0.053	0.409	0.076	0.293	--
20	0.006	0.047	0.004	0.016	--
21	0.039	0.296	0.053	0.203	--
22	0.003	0.022	0.012	0.046	--
23	0.028	0.217	0.037	0.143	--
24	0.001	0.011	0.007	0.026	--
25	0.019	0.147	0.029	0.111	--
26	0.003	0.022	0.003	0.011	--
27	0.012	0.090	0.018	0.070	--
28	0.001	0.006	0.004	0.016	--
29	0.012	0.091	0.008	0.029	--
30	0.001	0.011	0.009	0.033	--
31	0.011	0.087	0.011	0.043	--
32	0.002	0.014	0.005	0.021	--
33	0.009	0.066	0.011	0.042	--
34	0.006	0.045	0.006	0.025	--
35	0.010	0.074	0.009	0.033	--
36	0.002	0.017	0.002	0.007	--
37	0.010	0.080	0.009	0.034	--
38	0.002	0.017	0.003	0.010	--
39	0.010	0.074	0.008	0.030	--
40	0.013	0.097	0.000	0.001	--
THD (%)	0.311	2.914	0.590	2.267	13
PWHD (%)	0.572	4.377	0.770	2.958	22

Current Harmonics



THD & PWHD



4.2.2 Power Factor

The test was performed according to the point 13.8.4.2 of the standard.

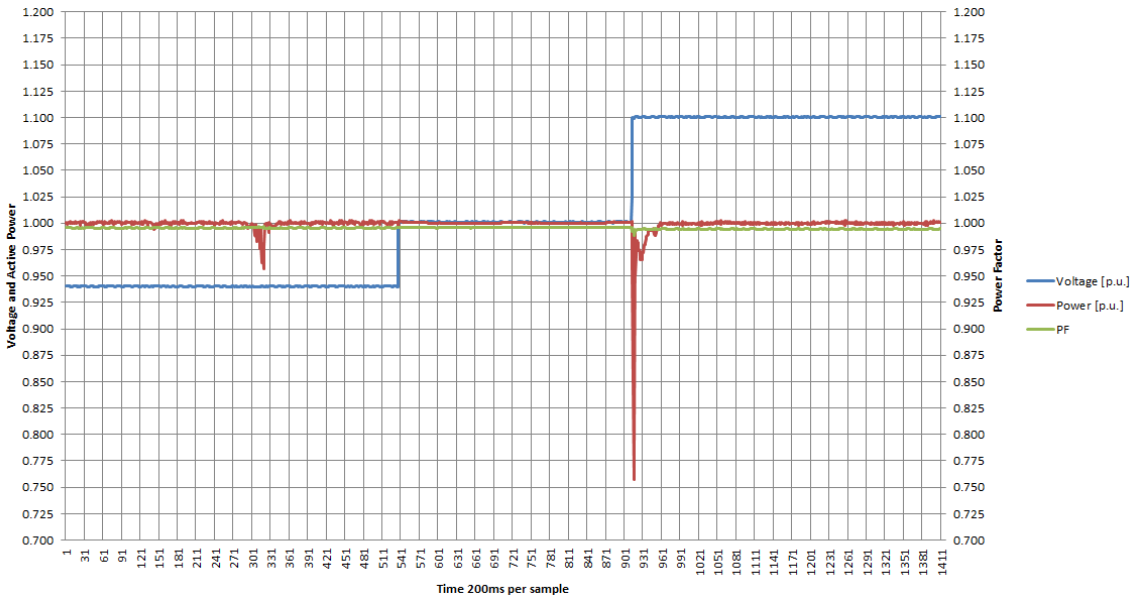
The power factor was measured at three voltage levels at rated power. The voltage was maintained within ±1.5% of the stated level during the test.

The following table shows the test results at different voltage levels:

Power Fixed					
Voltage required (p.u)	**Voltage measured (p.u)**	**PF required**	**PF measured**	**Active Power required (p.u)**	**Active Power measured (p.u)**
0,940	0.940	>0,95	0.995	1,000	1.001
1,000	1.001	>0,95	0.996	1,000	1.000
1,100	1.101	>0,95	0.995	1,000	1.000

Test results are graphically shown below.

Maximum Power Factor Fixed



4.2.3 Voltage Flicker

This test has been performed according to the point 13.8.4.3 and regarding the procedures specified by BS EN 61000-3-3.

Test results offered have a reference grid impedance of 30º

The measurements of voltage fluctuations have been measured according to the standard, at 33%, 66% and 100 % of the nominal power value of the inverter.

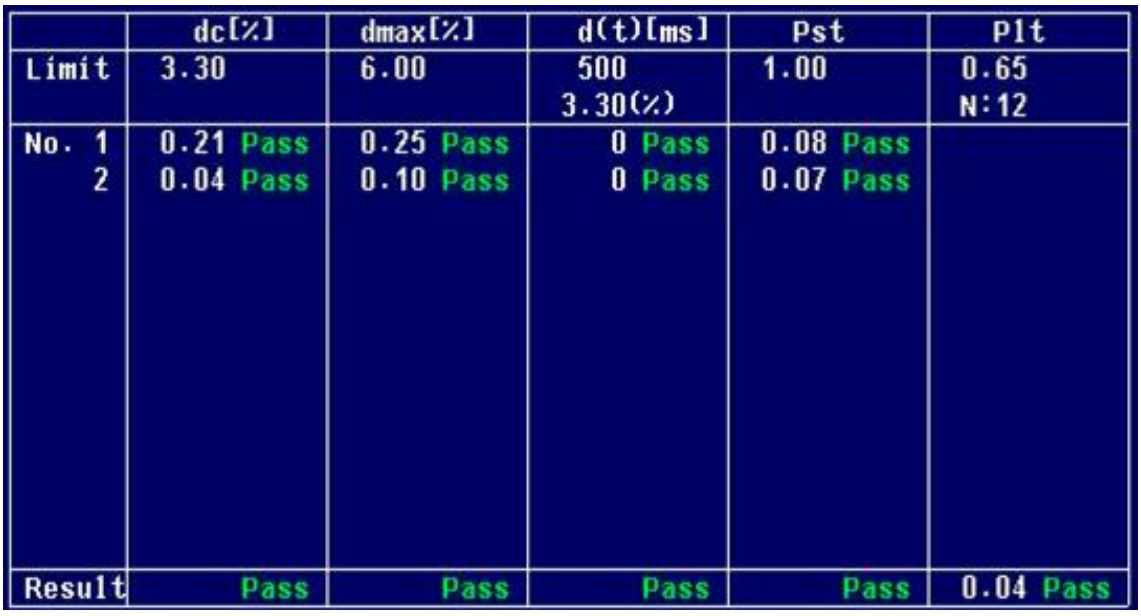
Starting operation and Stopping operation				
Pbin (%)	**Limit**	**33 %**	**66 %**	**100 %**
PST	≤ 1	0.08	0.10	0.12
PLT	≤ 0.65	0.04	0.05	0.06
dc	≤ 3.30%	0.21	0.35	0.48
dmax	4%	0.25	0.54	0.81

As it can be seen in the next screenshots, this test has two steps:

1. Starting operation
2. Stopping operation

All values are the most unfavorable of the two steps.

Starting operation and Stopping operation
33% Pn



	dc[%]	dmax[%]	d(t)[ms]	Pst	Plt
Limit	3.30	6.00	500 3.30(%)	1.00	0.65 N:12
No. 1	0.21 Pass	0.25 Pass	0 Pass	0.08 Pass	
2	0.04 Pass	0.10 Pass	0 Pass	0.07 Pass	
Result	Pass	Pass	Pass	Pass	0.04 Pass

66% Pn

	dc[%]	dmax[%]	d(t)[ms]	Pst	P1t
Limit	3.30	6.00	500 3.30(%)	1.00	0.65 N:12
No. 1	0.35 Pass	0.54 Pass	0 Pass	0.10 Pass	
2	0.11 Pass	0.15 Pass	0 Pass	0.08 Pass	
Result	Pass	Pass	Pass	Pass	0.05 Pass

100% Pn

	dc[%]	dmax[%]	d(t)[ms]	Pst	P1t
Limit	3.30	6.00	500 3.30(%)	1.00	0.65 N:12
No. 1	0.48 Pass	0.81 Pass	0 Pass	0.12 Pass	
2	0.11 Pass	0.14 Pass	0 Pass	0.08 Pass	
Result	Pass	Pass	Pass	Pass	0.06 Pass

Running operation				
Pbin (%)	**Limit**	**33 %**	**66 %**	**100 %**
PST	≤ 1	0.08	0.11	0.07
PLT	≤ 0.65	0.08	0.10	0.07
dc	≤ 3.30%	0.24	0.44	0.00
dmax	4%	0.30	0.60	0.00

As it can be seen in the next screenshots is running operation. The values took of Pst and Plt are the most unfavorable of the twelve steps.

Running operation

33% Pn

	dc[%]	dmax[%]	d(t)[ms]	Pst	Plt
Limit	3.30	6.00	500 3.30(%)	1.00	0.65 N:12
No. 1	0.20 Pass	0.30 Pass	0 Pass	0.08 Pass	
2	0.17 Pass	0.30 Pass	0 Pass	0.08 Pass	
3	0.24 Pass	0.29 Pass	0 Pass	0.08 Pass	
4	0.16 Pass	0.24 Pass	0 Pass	0.08 Pass	
5	0.21 Pass	0.22 Pass	0 Pass	0.08 Pass	
6	0.24 Pass	0.24 Pass	0 Pass	0.08 Pass	
7	0.19 Pass	0.28 Pass	0 Pass	0.08 Pass	
8	0.18 Pass	0.29 Pass	0 Pass	0.08 Pass	
9	0.12 Pass	0.27 Pass	0 Pass	0.08 Pass	
10	0.20 Pass	0.21 Pass	0 Pass	0.08 Pass	
11	0.15 Pass	0.25 Pass	0 Pass	0.08 Pass	
12	0.21 Pass	0.25 Pass	0 Pass	0.08 Pass	
Result	Pass	Pass	Pass	Pass	0.08 Pass

66% Pn

	dc[%]	dmax[%]	d(t)[ms]	Pst	P1t
Limit	3.30	6.00	500 3.30(%)	1.00	0.65 N:12
No. 1	0.35 Pass	0.54 Pass	0 Pass	0.10 Pass	
2	0.34 Pass	0.57 Pass	0 Pass	0.10 Pass	
3	0.35 Pass	0.52 Pass	0 Pass	0.10 Pass	
4	0.39 Pass	0.53 Pass	0 Pass	0.10 Pass	
5	0.41 Pass	0.58 Pass	0 Pass	0.10 Pass	
6	0.34 Pass	0.57 Pass	0 Pass	0.10 Pass	
7	0.42 Pass	0.56 Pass	0 Pass	0.11 Pass	
8	0.13 Pass	0.16 Pass	0 Pass	0.08 Pass	
9	0.44 Pass	0.60 Pass	0 Pass	0.10 Pass	
10	0.42 Pass	0.48 Pass	0 Pass	0.10 Pass	
11	0.35 Pass	0.50 Pass	0 Pass	0.10 Pass	
12	0.41 Pass	0.52 Pass	0 Pass	0.10 Pass	
Result	Pass	Pass	Pass	Pass	0.10 Pass

100% Pn

	dc[%]	dmax[%]	d(t)[ms]	Pst	P1t
Limit	3.30	6.00	500 3.30(%)	1.00	0.65 N:12
No. 1	0.00 Pass	0.00 Pass	0 Pass	0.07 Pass	
2	0.00 Pass	0.00 Pass	0 Pass	0.07 Pass	
3	0.00 Pass	0.00 Pass	0 Pass	0.07 Pass	
4	0.00 Pass	0.00 Pass	0 Pass	0.07 Pass	
5	0.00 Pass	0.00 Pass	0 Pass	0.07 Pass	
6	0.00 Pass	0.00 Pass	0 Pass	0.07 Pass	
7	0.00 Pass	0.00 Pass	0 Pass	0.07 Pass	
8	0.00 Pass	0.00 Pass	0 Pass	0.07 Pass	
9	0.00 Pass	0.00 Pass	0 Pass	0.07 Pass	
10	0.00 Pass	0.00 Pass	0 Pass	0.07 Pass	
11	0.00 Pass	0.00 Pass	0 Pass	0.07 Pass	
12	0.00 Pass	0.00 Pass	0 Pass	0.07 Pass	
Result	Pass	Pass	Pass	Pass	0.07 Pass

4.2.4 DC Injection

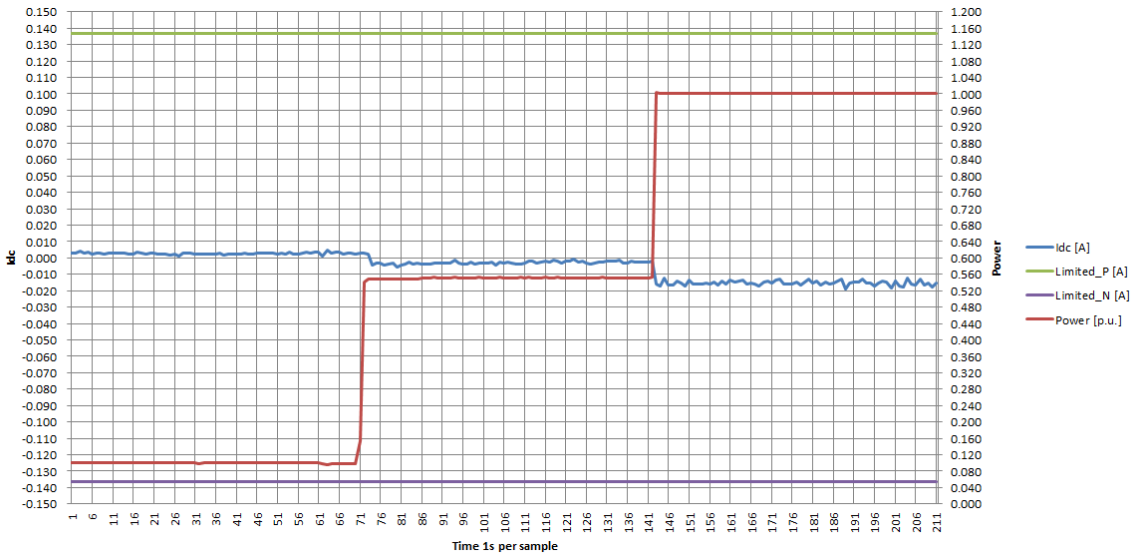
The evaluation of this point has been made according to the point 13.8.4.4 of the standard.

This test does not apply because the output of the inverter has to be connected to an external transformer.

The DC current must be smaller than 136.5 mA.

(25±5ºC)			
	Min ~ 33% Pn	**Medium ~ 66% Pn**	**Max ~ 100% Pn**
Test value (mA)	4.6	5.3	18.9

DC injection test result



4.2.5 Self Monitoring solid state distribution

The evaluation of this point has been made according to the point 13.8.4.7 of the standard.

This test does not apply because in the inverter there are not solid-state switching devices.

4.2.6 Short circuit current contribution

The test was performed according to the point 13.8.4.6 of the standard.

They have been performed different short circuit tests that are detailed in the table and pictures below.

Short circuit current			
Short Circuit Applied	**Time after fault**	**Volts(V)**	**Amps(A)**
Line to neutral	20ms	1.92	23.82
Line to neutral	100ms	1.75	20.34
Line to neutral	250ms	0.04	0.23
Line to neutral	500ms	0.25	0.08
Line to neutral	Time to trip	0.13	In seconds

Time after 20ms fault

Voltage:

Current

Time after 100ms fault

Voltage:

Current

Time after 250ms fault

Voltage:

Current

Time after 500ms fault

Voltage:

Current

Time to trip

4.2.7 Electromagnetic Compatibility

The compliances with these requirements is stated in the following test report:

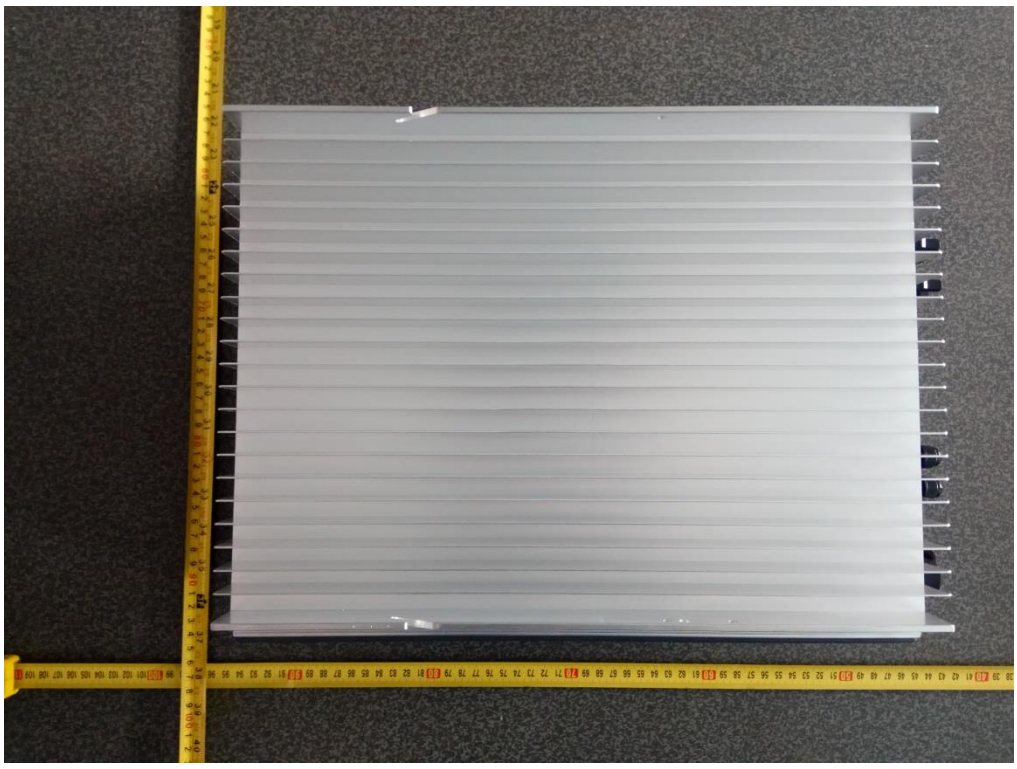
According to the EU Declaration of Conformity issued by Schneider Electric, equipments under the scope of this test report meet the requirements of EMC directive 2014/30/UE and Low Voltage Directive 2014/35/EU. See point 7 of this report.

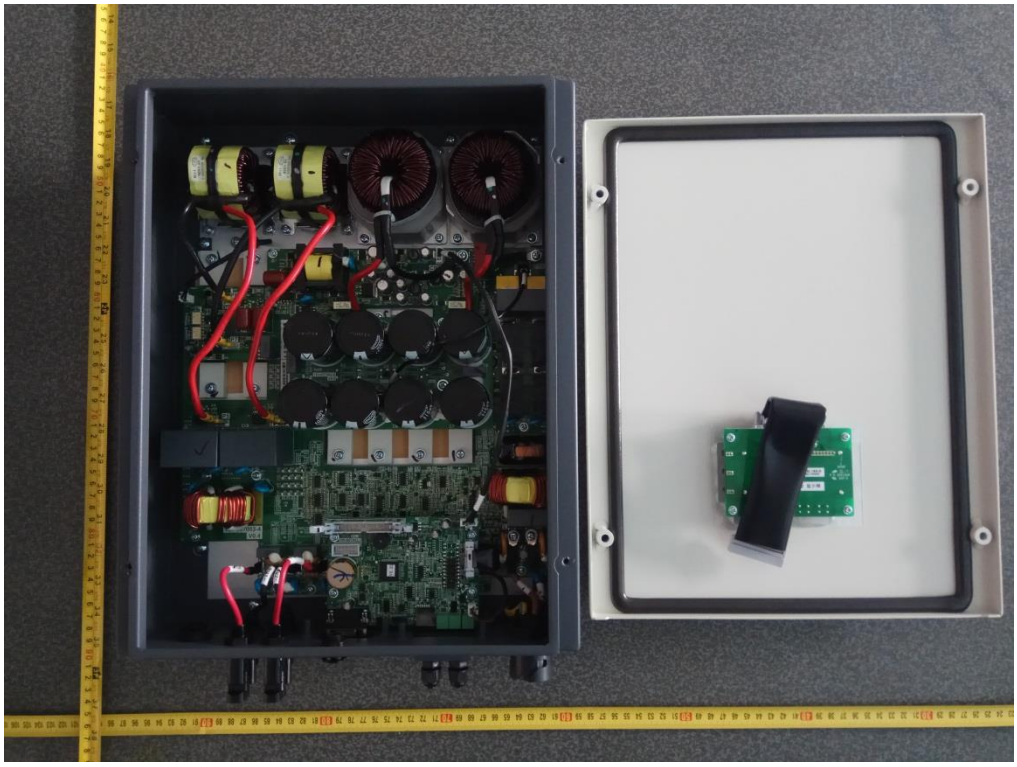
5 PICTURES

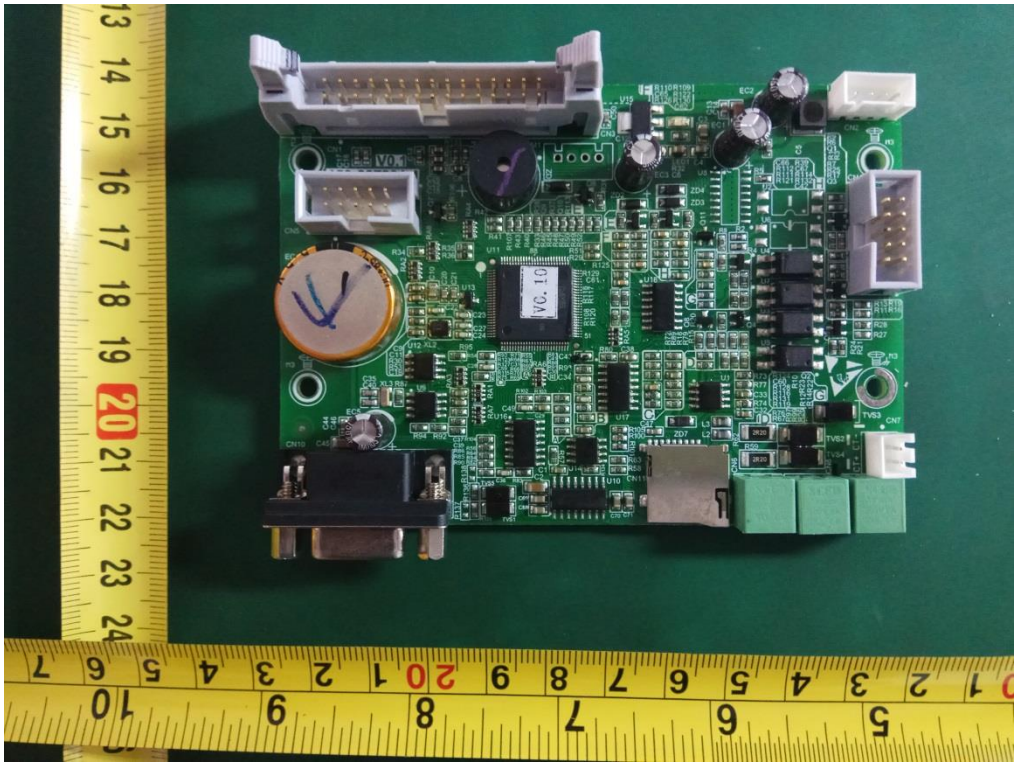
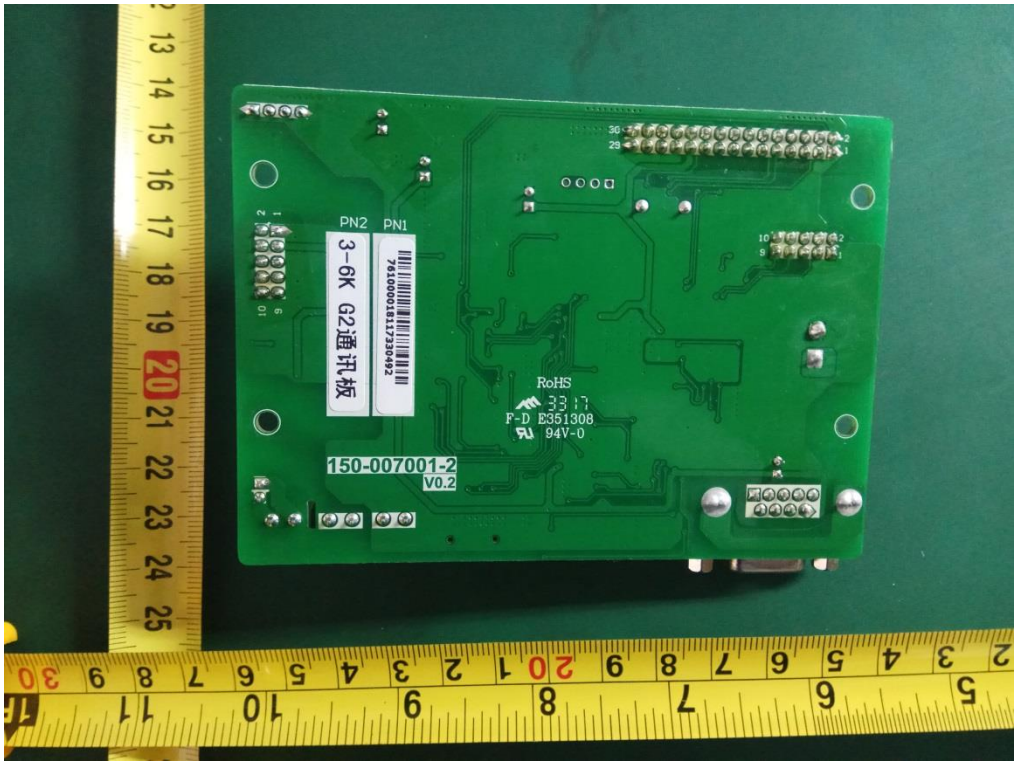
Front

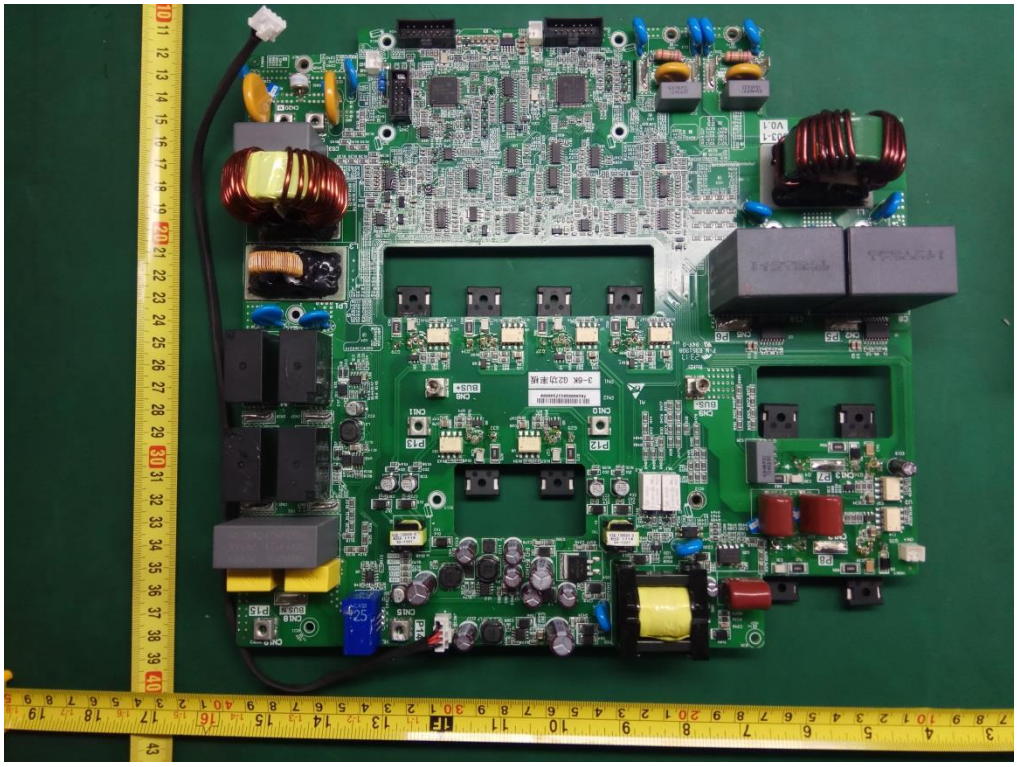
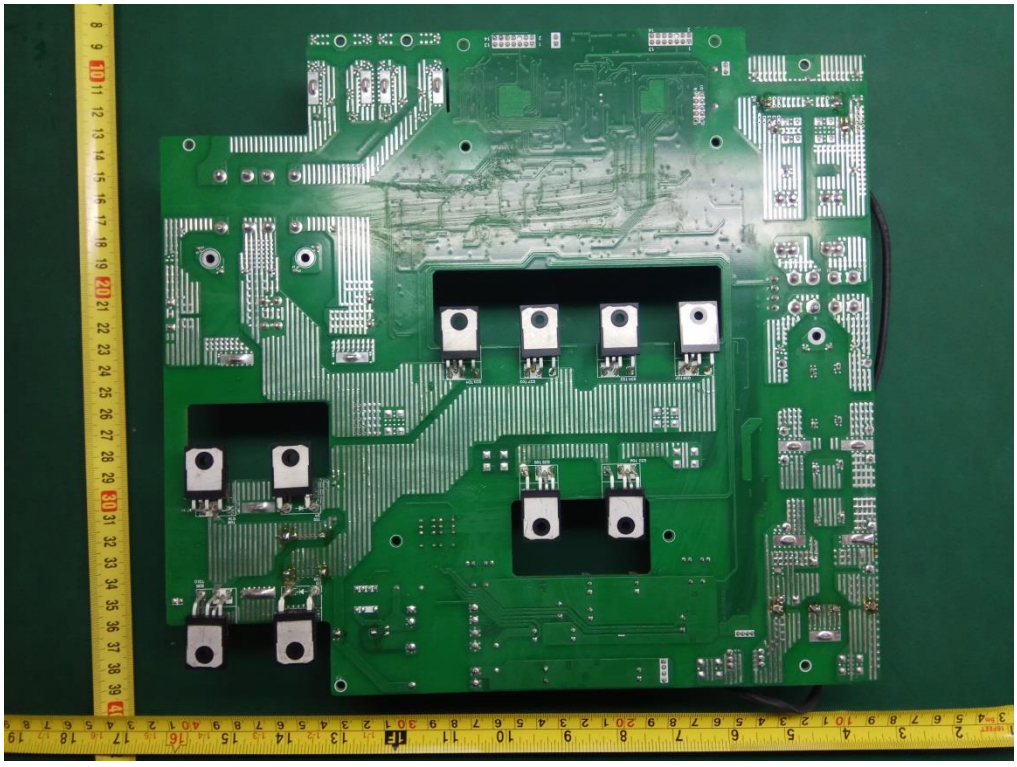
Side

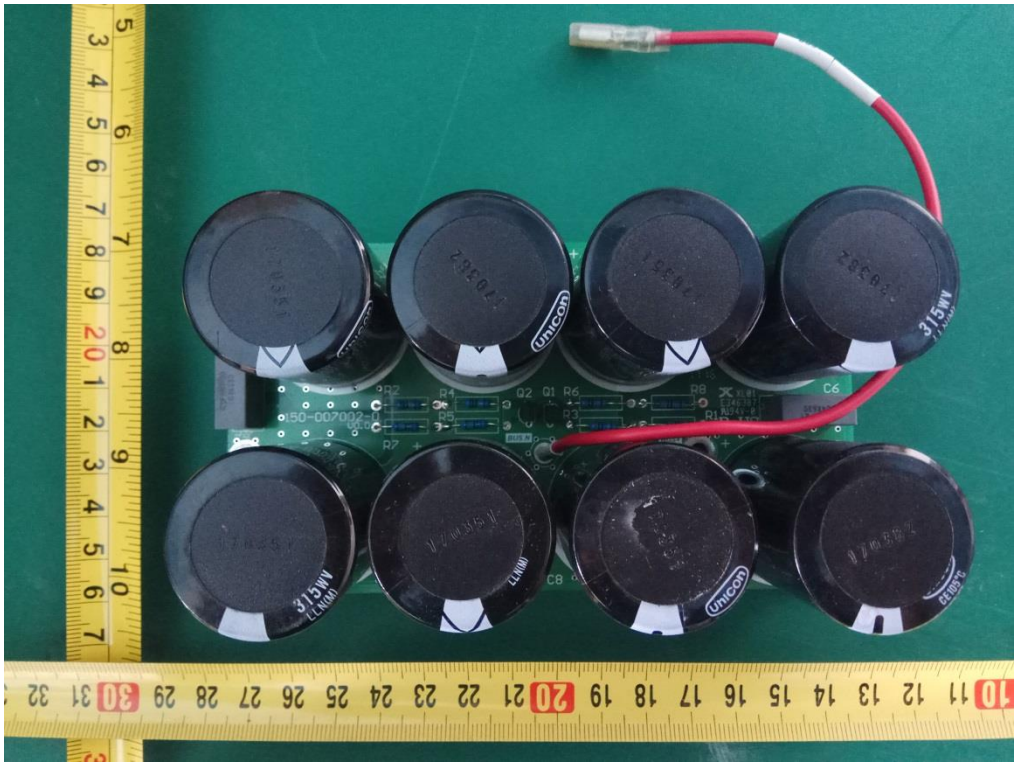
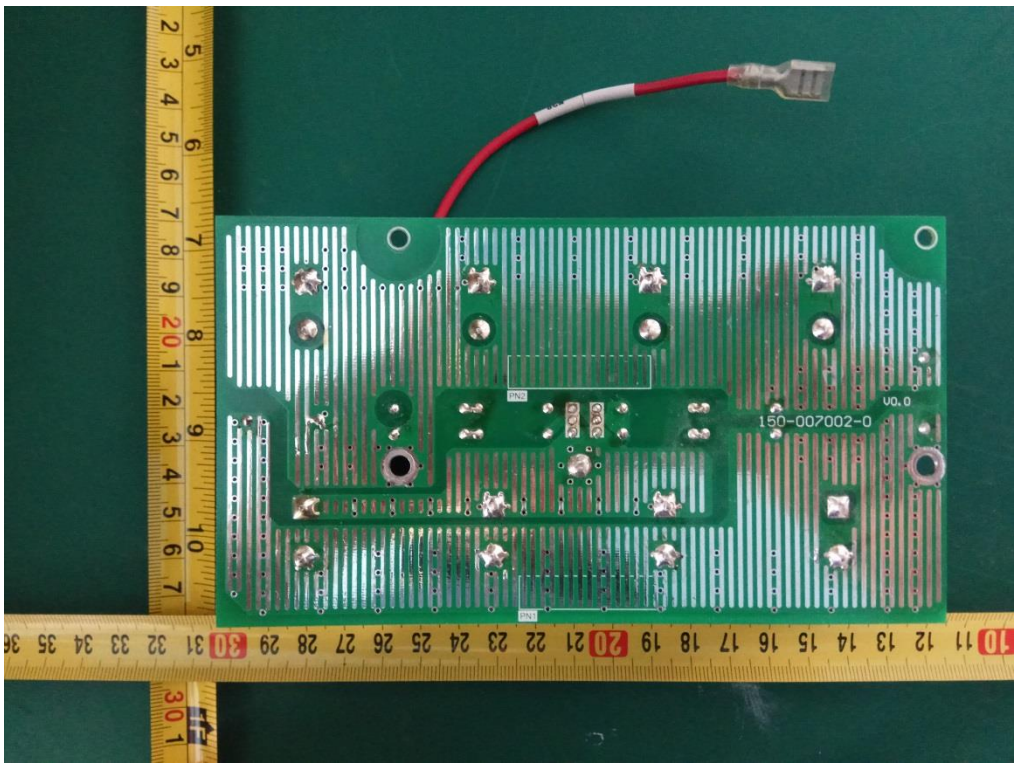

Connection interface

Back Side


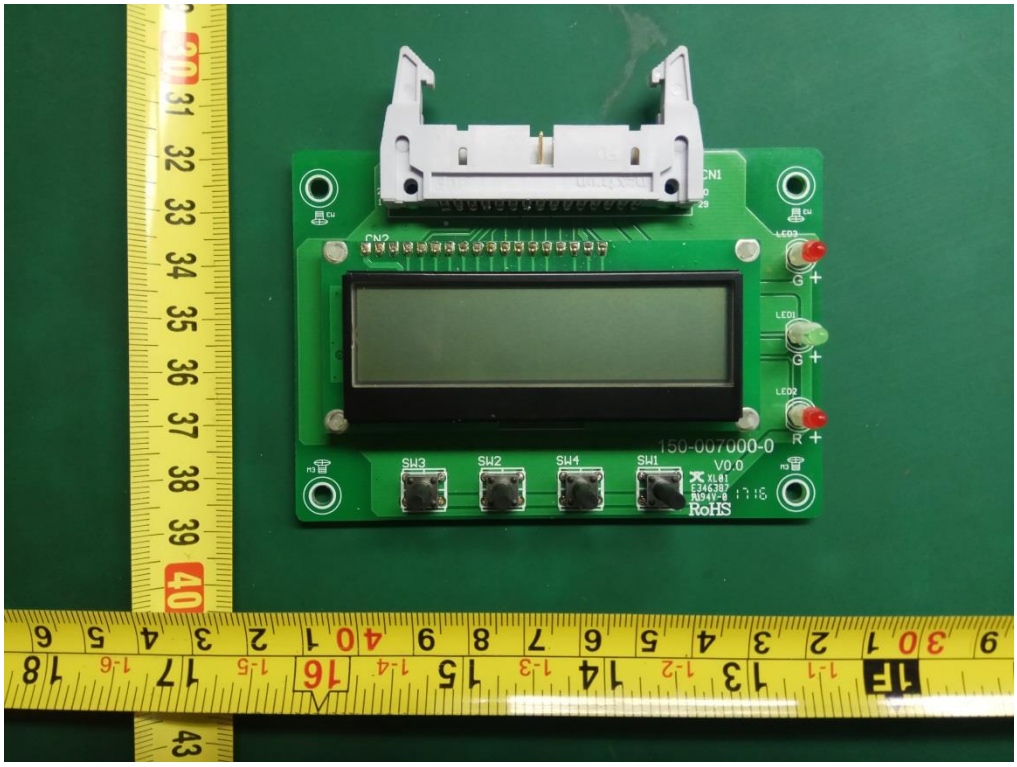
Internal

Internal


Front side of communication baord

Back side of communication baord


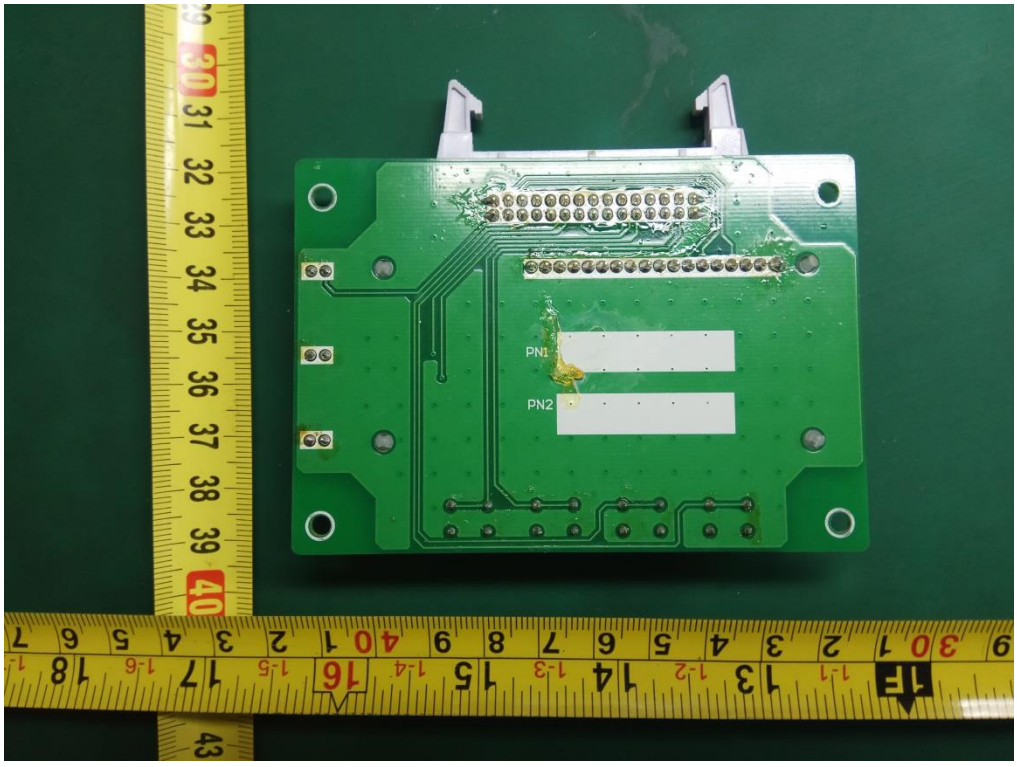
Front side of Main board

Front side of Main board


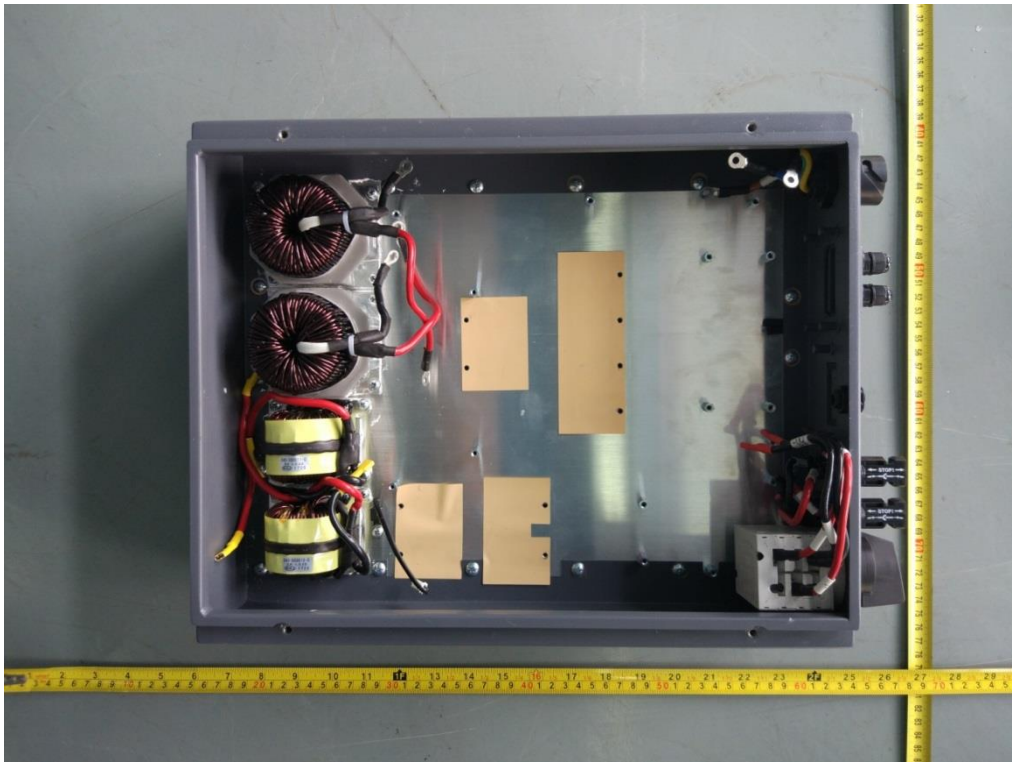
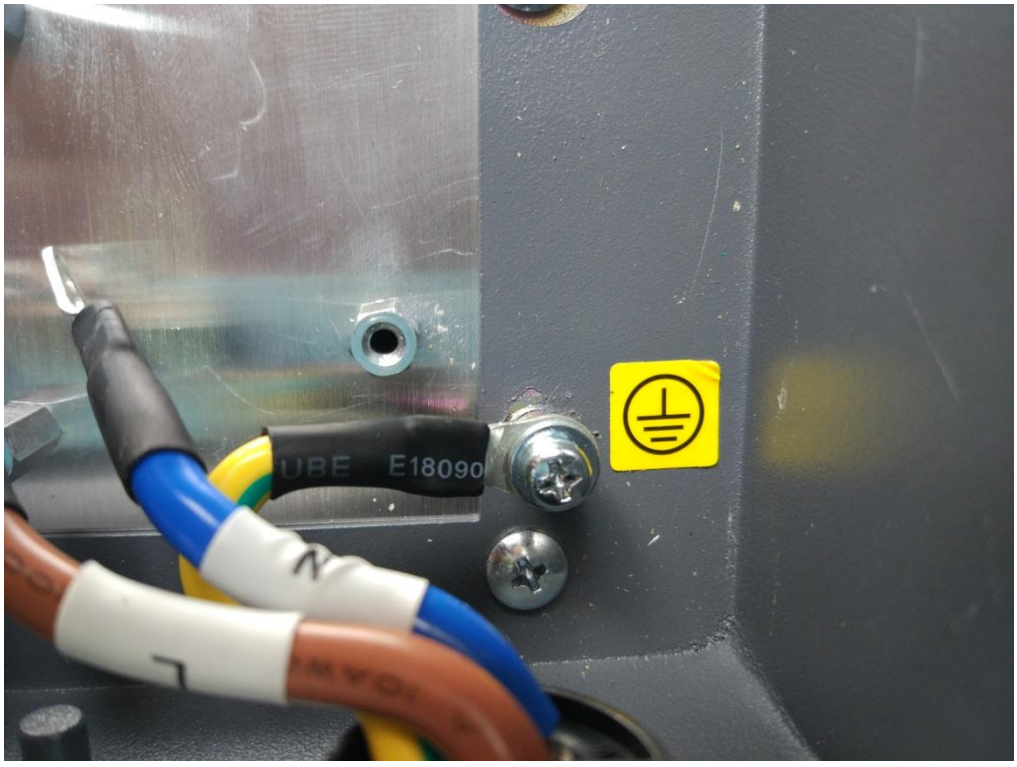
Front side of Bus capacitors board

Back side of Bus capacitors board


Front side of display board

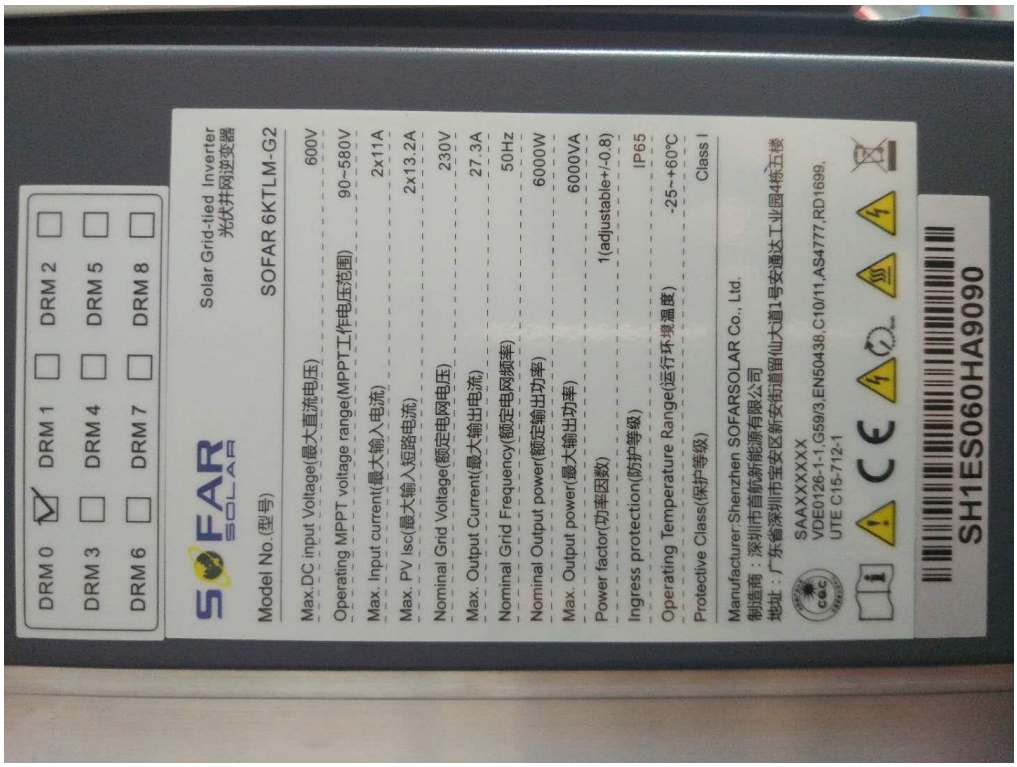


Back side of display board

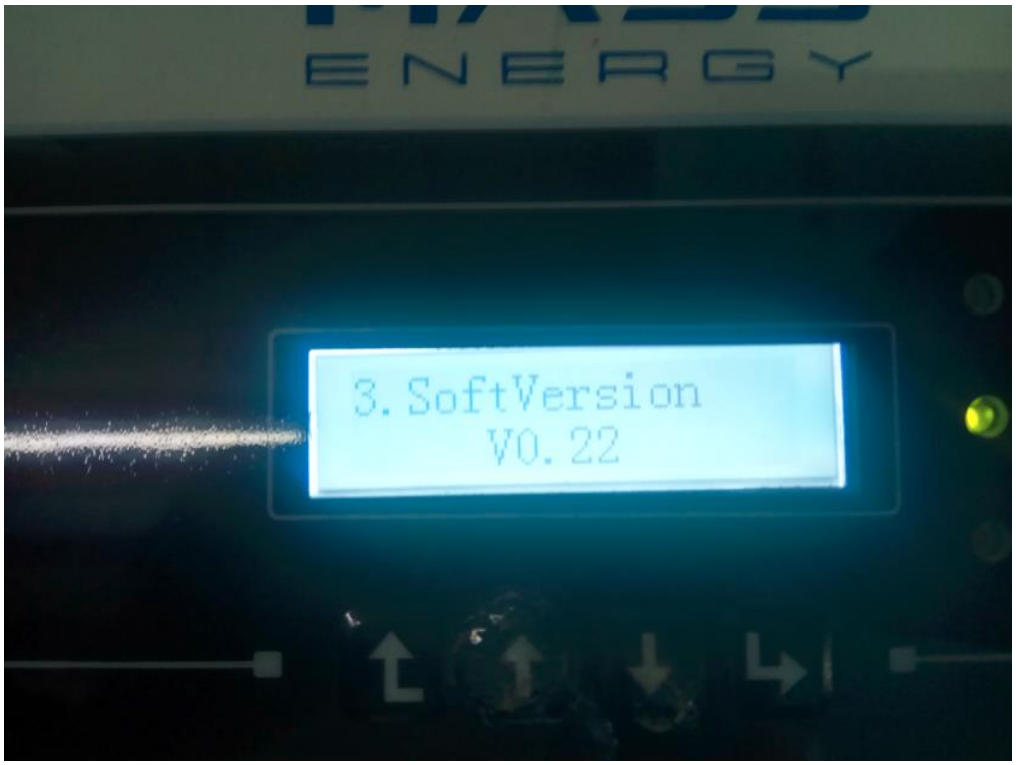


Removed all PCBAs

Cover


Labels



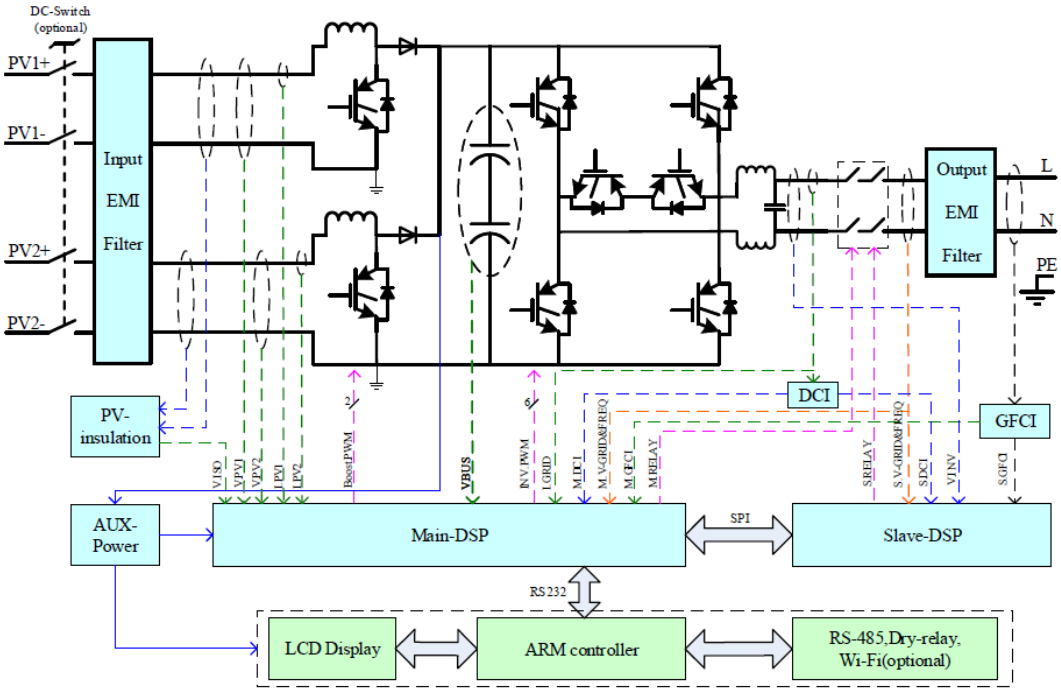
Software Version



Serial Number of the EUT


6 ELECTRICAL SCHEMES

Equipment under testing



7 CE CONFORMITY CERTIFICATE

BUREAU VERITAS

ATTESTATION
of conformity with European Directives

Attestation Number:	1788AB0829N003001
Product:	Solar Inverter
Brand Name:	SOFAR SOLAR
Model:	SOFAR 6KTLM-G2, SOFAR 3KTLM-G2
Additional Model:	SOFAR 5KTLM-G2, SOFAR 4.6KTLM-G2, SOFAR 4KTLM-G2, SOFAR 3.6KTLM-G2
Applicant:	Shenzhen SOFAR SOLAR Co., Ltd.
Address:	5/F,Building 4, Antongda Industrial Park, No.1 Liuxian Avenue,Xin'an Street,Bao'an District, Shenzhen City, Guangdong Province,P.R. China.
Technical Characteristics:	DC input 90-580V AC output 220-230V 50/60Hz

The submitted sample of the above equipment has been tested for CE marking according to following European Directive and following standards:

- **Electromagnetic Compatibility Directive 2014/30/EU**

Standards	Report Number	Report date
EN 61000-6-3:2007 + A1:2011 EN 61000-3-2:2014 EN 61000-3-3:2013 EN 61000-3-11:2001 EN 61000-3-12:2011 EN 61000-6-2:2005	CE170829N003	Dec. 08, 2017

The referred test report(s) show that the product complies with standard(s) recognized as giving presumption of compliance with the essential requirements in the specified European Directive.

This verification does not imply assessment of the production of the product. The CE marking may be affixed if all relevant and effective European Directives with CE are applicable.

CE

Supervisor
EMC Department

Name: Madison Luo
Date: Dec. 08, 2017

Bureau Veritas Shenzhen Co., Ltd. Dongguan Branch

No. 34, Chenwulu Section, Guantai Rd., Houjie Town, Dongguan City, Guangdong 523942, China

Tel.: +86 769 8593 5656
Fax: +86 769 8593 1080
Email:customerservice.dg@cn.bureauveritas.com

Attestation of Conformity

AOC No.:	**1788AP0829N003**
Equipment:	**Solar Grid-tied inverter**
Brand Name:	**SOFAR SOLAR**
Test Model No.:	**SOFAR 6KTLM-G2, SOFAR 5KTLM-G2, SOFAR 4.6KTLM-G2, SOFAR 4KTLM-G2, SOFAR 3.6KTLM-G2, SOFAR 3KTLM-G2**
Applicant:	**Shenzhen Sofarsolar Co.,Ltd 5/F, Building 4, Antongda Industrial Park, No.1 Liuxian Avenue, Xin'an Street, Bao'an District, Shenzhen City, Guangdong Province, P.R. China**
Report No.:	**LD170829N003**

The submitted sample of the above equipment has been tested for CE marking according to following European Directive and standards:

- **Low Voltage Directive 2014/35/EU.**

The referred test report(s) show that the product complies with standard(s) recognized as giving presumption of compliance with the essential requirements in the specified European Directive.

This verification does not imply assessment of the production of the product. The CE marking may be affixed if all relevant and effective European Directives with CE are applicable.

Applied rules and standards
IEC/EN 62109-1:2010
Safety of power converters for use in photovoltaic power systems – Part 1: General requirements
IEC/EN 62109-2:2011
Safety of power converters for use in photovoltaic power systems –
Part 2: Particular requirements for inverters

Name: Ted Wu
Senior Manager/ PV Inverter Team
Date: 2017-08-18

Bureau Veritas Shenzhen Co., Ltd. Dongguan Branch
No. 34, Chenwulu Section, Guantai Rd., Houjie Town, Dongguan City, Guangdong 523942, China.
Tel: +86 769 8593 5656; Fax: +86 769 8593 1080.
Email: customerservice.dg@cn.bureauveritas.com

----------END OF REPORT----------